

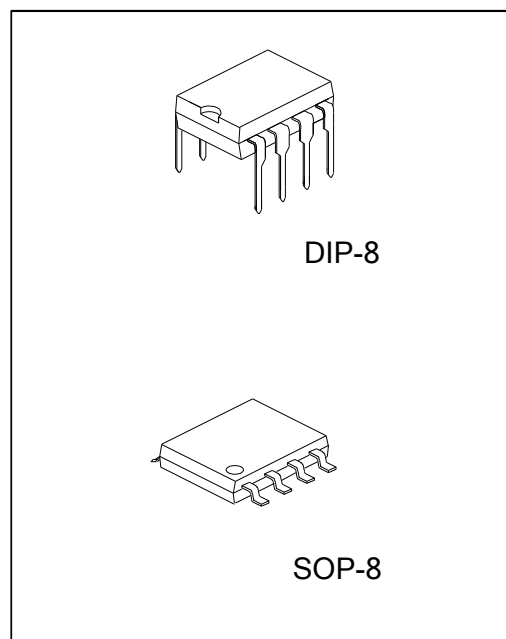
CURRENT MODE PWM CONTROL CIRCUITS

DESCRIPTION

The UC3844 provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N channel MOSFETs, is low in the off state.

FEATURES

- * Optimized for off-line and DC to DC converts
- * Low start up current(<0.5mA)
- * Automatic feed forward compensation
- * Pulse-by-Pulse current limiting
- * Enhanced load response characteristics
- * Under-voltage lockout with hysteresis
- * Double pulse Suppression
- * High current totem pole output
- * Internally trimmed bandgap reference
- * 500kHz operation
- * Low Ro error amp



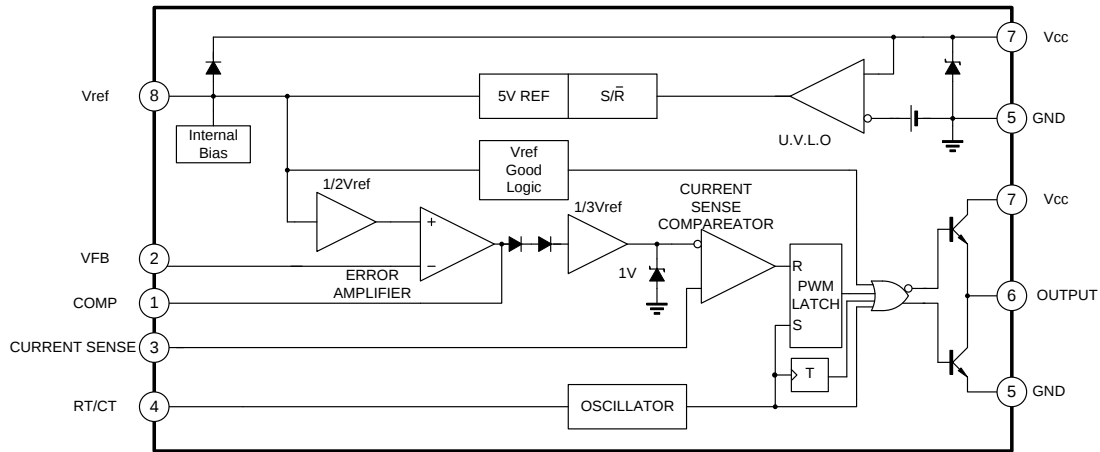
ORDERING INFORMATION

Ordering Number	Package	Free	Packing
UC3844-D8	DIP-8	RoHS	Tube
UC3844-P8	SOP-8	RoHS	Tape Reel



UC3844

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage(Low Impedance Source)	V _{CC}	30	V
Supply Voltage(I _{CC} <30mA)	V _{CC}	Self Limiting	V
Output Current	I _O	±1	A
Output Energy(capacitive Load)		5	μJ
Analog Inputs(pin 2,3)	V _{I(ANA)}	-0.3 to +6.3	V
Error Amplifier Output Sink Current	I _{SINK(EA)}	10	mA
Power Dissipation at T _{amb} ≤25°C	P _D	DIP-8	1.0
		SOP-8	0.75
Lead Temperature(10 sec)	T _{lead}	260	°C
Storage Temperature	T _{stg}	-65 ~ +150	°C
Junction Operating Temperature	T _J	+150	°C

Note 1: Ta>25°C,P_D derated with 8mW/°C.

ELECTRICAL CHARACTERISTICS (0≤Ta≤70°C,V_{CC}=15V,R_T=10kΩ,C_T=3.3nF,unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Section						
Output Voltage	V _{REF}	T _J =25°C,I _O =1mA	4.90	5.00	5.10	V
Line Regulation	ΔV _{REF}	12≤V _{IN} ≤25V		2	20	mV
Load Regulation	ΔV _{REF}	1≤I _O ≤20mA		3	25	mV
Temperature Stability		(Note 2)		0.2		mV/°C
Total Output Variation		Line,Load,Temp(note 2)	4.82		5.18	V
Output Noise Voltage	e _N	10Hz≤f≤10kHz,T _J =25°C (note 2)		50		μV
Long term stability		Ta=25°C,1000Hrs(note 2)		5	25	mV
Output Short Circuit	I _{SC}		-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f _{osc}	T _J =25°C	49	52	55	kHz
Voltage Stability	Δf/ΔV _{CC}	12≤V _{CC} ≤25V		0.2	1	%
Temp stability		T _{min} ≤Ta≤T _{max} (note 2)		5		%
Amplitude	V _{osc}	V _{pin 4} peak to peak		1.6		V



(continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Error Amplifier Section						
Input Voltage	$V_{I(EA)}$	$V_{pin\ 1}=2.5V$	2.42	2.50	2.58	V
Input Bias current	I_{BIAS}			-0.1	-2	μA
AVOL		$2 \leq V_o \leq 4V$	60	90		dB
Unity Gain Bandwidth		$T_j=25^\circ C$ (note 2)	0.7	1		MHz
PSRR		$I_2 \leq V_{cc} \leq 25V$	60	70		dB
Output Sink Current	I_{sink}	$V_{pin\ 2}=2.7V, V_{pin\ 1}=1.1V$	2	12		mA
Output Source Current	I_{source}	$V_{pin\ 2}=2.3V, V_{pin\ 1}=5V$	-0.5	-1		mA
Vout High		$V_{pin\ 2}=2.3V, R_L=15k\Omega$ to GND	5	6.2		V
Vout Low		$V_{pin\ 2}=2.7V, V_{pin\ 1}=1.1V$		0.8	1.1	V
Current Sense section						
Gain	G_V	(note 3,4)	2.85	3	3.15	V/V
Maximum Input signal	$V_{I(MAX)}$	$V_{pin\ 1}=5V$ (note 3)	0.9	1	1.1	V
SVR		$12 \leq V_{cc} \leq 25V$		70		dB
Input Bias Current	I_{BIAS}			-2	-10	μA
Delay to Output		$V_{pin\ 3}=0$ to 2V		150	300	ns
Output Section						
Output low Level	V_{OL}	$I_{sink}=20mA$		0.1	0.4	V
		$I_{sink}=200mA$		1.6	2.2	V
Output High Level	V_{OH}	$I_{source}=20mA$	13	13.5		V
		$I_{source}=200mA$	12	13.5		V
Rise Time	t_R	$T_j=25^\circ C, C_L=1nF$ (note 2)		50	150	ns
Fall Time	t_F	$T_j=25^\circ C, C_L=1nF$ (note 2)		50	150	ns
UVLO Saturation		$V_{cc}=5V, I_{sink}=10mA$		0.7	1.2	V
Under-Voltage Lockout Output Section						
Start Threshold	$V_{TH(ST)}$		14.5	16	17.5	V
Min.Operating Voltage After Turn On	$V_{OPR(min)}$		8.5	10	11.5	V
PWM Section						
Maximum duty Cycle	$D_{(MAX)}$		47	48	50	%
Minimum Duty Cycle	$D_{(MIN)}$				0	%
Total Standby Current						
Start-up Current	I_{ST}			0.3	0.5	mA
Operating Supply Current	$I_{CC(opr)}$	$V_{pin\ 2}=V_{pin\ 3}=0V$		12	17	mA
Vcc Zener Voltage	V_Z	$I_{cc}=25mA$		34		V

note 2: These parameters, although guaranteed, are not 100% tested in production.

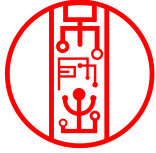
note 3: Parameters measured at trip point of latch with $V_{pin\ 2}=0$.

note 4: Gain defined as:

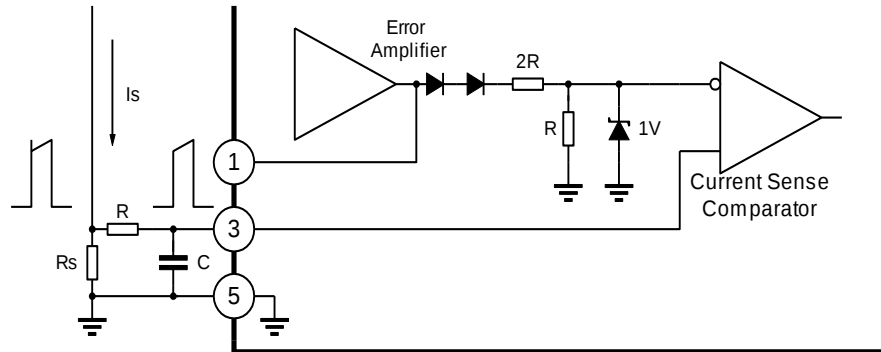
$$A = \frac{\Delta V_{pin\ 1}}{\Delta V_{pin\ 3}} ; 0 \leq V_{pin\ 3} \leq 0.8V$$

note 5: Adjust V_{cc} above the start threshold before setting at 15V.





CURRENT SENSE CIRCUIT

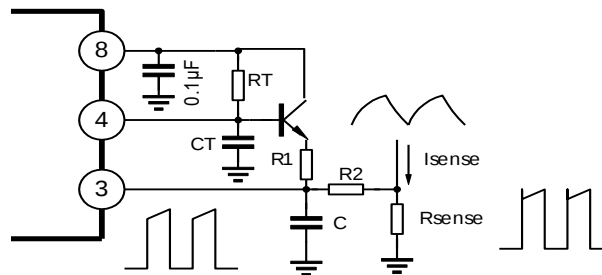


Peak current (I_s) determined by the formula:

$$I_{smax} = 10V / R_s$$

A small RC filter be required to suppress switch transients.

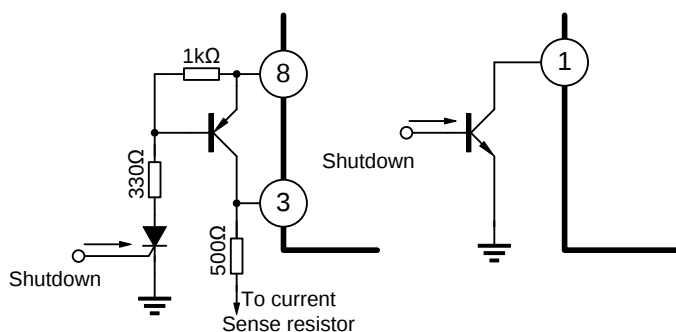
SLOPE COMPENSATION



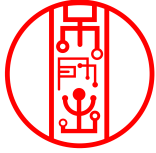
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over

50%. Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.

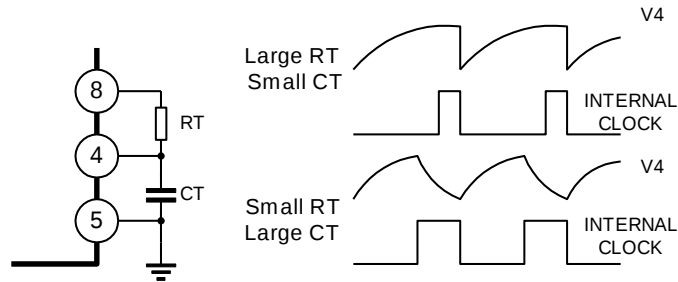
SHUTDOWN TECHNIQUES



Shutdown UC3844 can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which be reset by cycling V_{cc} below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.



OSCILLATOR SECTION



Deadtime VS C_T ($R_T > 5k\Omega$)

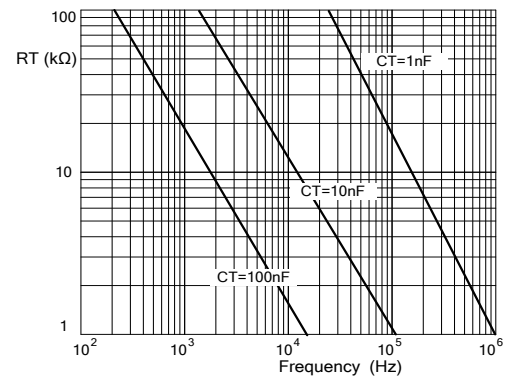
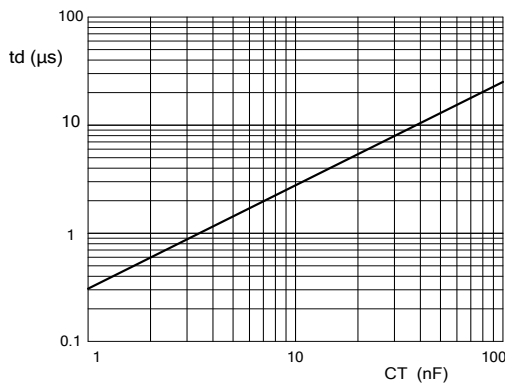
Timing Resistance Vs Frequency

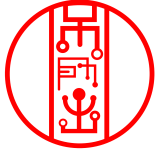
Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:
 $t_c = 0.625 R_T C_T$

$$t_D = R_T C_T \ln \left(\frac{0.0063 R_T - 2.7}{0.0063 R_T - 4} \right)$$

Frequency, then, is: $f = (t_c + t_d)^{-1}$

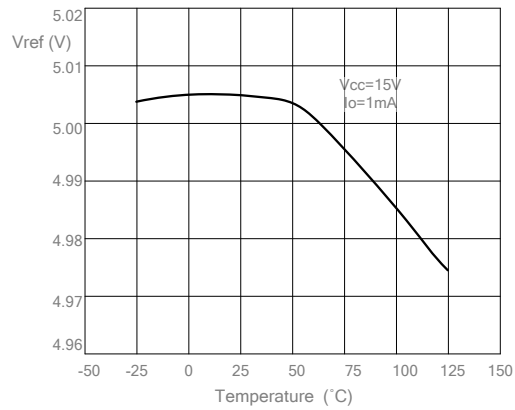
$$\text{For } R_T > 5k\Omega, f = \frac{1.6}{R_T C_T}$$



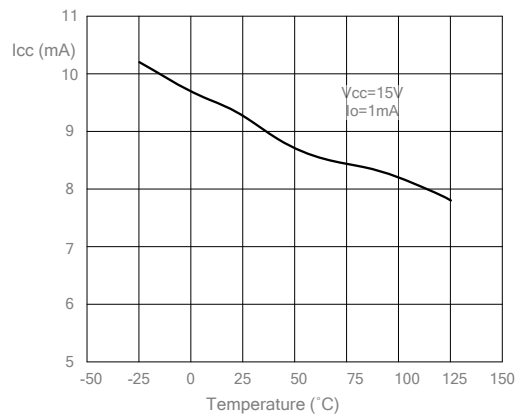
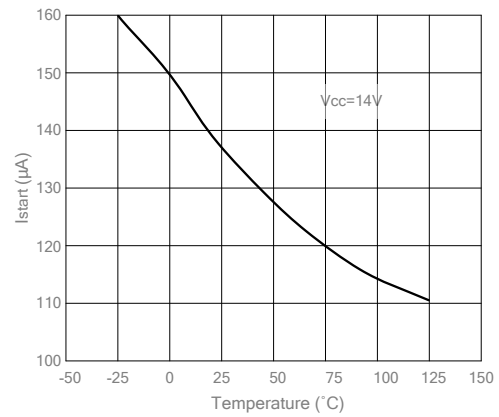


TYPICAL PERFORMANCE CHARACTERISTICS

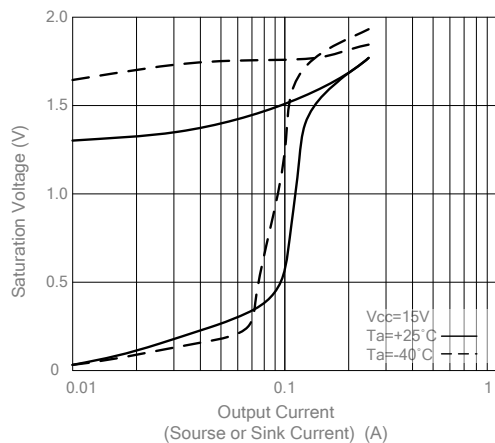
V_{ref} Temperature Drift



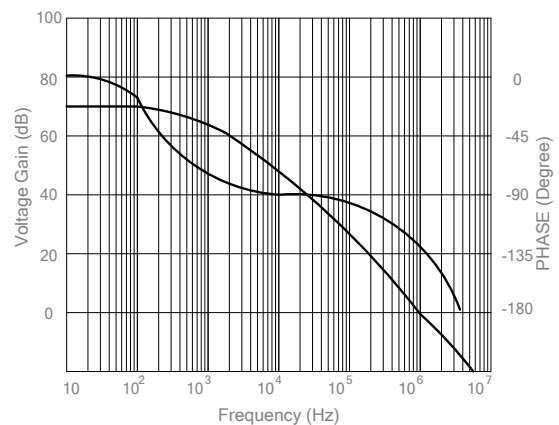
I_{start} Temperature Drift



I_{cc} Temperature Drift



Output Saturation Characteristics



Error Amplifier Open-Loop
Frequency Response