SKGM35N65-TL

Enhancement-mode GaN Power Transistor

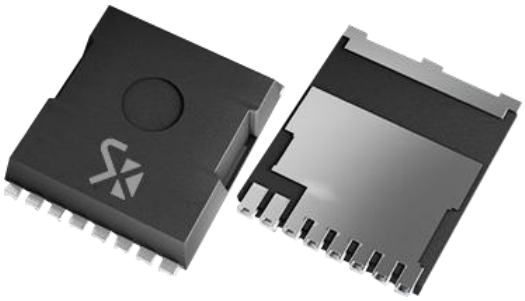
Key Performance Parameters at T_J=25℃		
Parameters	Values	Units
V_{DS},max	650	V
$R_{DS(on)}$,max	55	mΩ
Q_G,typ	6.5	nC
I_D,Pulse	60	A
Q_{OSS},@400V	60	nC
Q_{rr}	0	nC

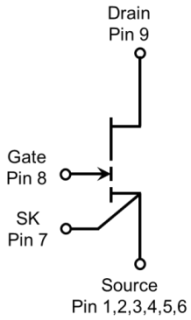
Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on)}$, max 55mΩ
- Recommended gate drive voltage 0V ~ 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3
- RoHS, Pb-free, REACH-compliant

Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- Wireless power transfer
- Power adapters, LED lighting drivers
- Laser drivers
- Industrial motor drives





Description

This is a 650V GaN-on-Si enhancement-mode power transistor in TO-Leadless (TOLL) package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.The TOLL package offers low parasitic resistance/inductance, strong heat dissipation and high solder ability, which can fully release device potential and make GaN better apply to industrial applications.

Ordering Information

Ordering Code	Package	Marking	Packing
	TOLL		Reel

Absolute Maximum Ratings(at T_J=25℃,unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-source voltage	$V_{DS,max}$	V_{GS} = 0 V; I_D = 10 μA			650	V
Drain-source voltage transient[1]	$V_{DS,transient}$	V_{GS} = 0 V; V_{DS} = 850 V			850	V
Continuous current, drain-source	I_D	T_C= 25 ℃			30	A

Pulsed current, drain-source [2]	$I_{D,pulse}$	T_C = 25 °C; V_G = 6 V			60	A
Pulsed current, drain-source [2]	$I_{D,pulse}$	T_C = 150 °C; V_G = 6 V			25	A
Gate-source voltage, continuous [3]	V_{GS}	T_J = -55 °C to 150 °C	+7		+7	V
Gate-source voltage, pulsed	$V_{GS,pulse}$	T_J = -55 °C to 150 °C; t_{Pulse} = 50 ns; f = 100 kHz; open drain	-20		+10	V
Power dissipation	P_{tot}	T_C = 25 °C			169	W
Operating temperature	T_J		-55		+150	°C
Storage temperature	T_{STG}		-55		+150	°C

1. V_{DS}, transient is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10 µs.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8

Thermal Characteristics

Parameter	Symbol	Notes/Test Condition	Values			Unit
			Min	Typ	Max	
Thermal resistance, junction-case	$R_{\theta JC}$				0.74	°C/W
Thermal resistance, junction-ambient [1]	$R_{\theta JA}$				40	°C/W
Reflow soldering temperature	T_{sold}	MSL3			260	°C

1. Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12mil) with 0.889 mm pitch (35mil). The copper layers under the thermal pad and drain pad are 25 * 25 mm^2each. The PCB is mounted in horizontal position without air stream cooling.

Electrical Characteristics(at T_J=25°C,unless otherwise specified.)

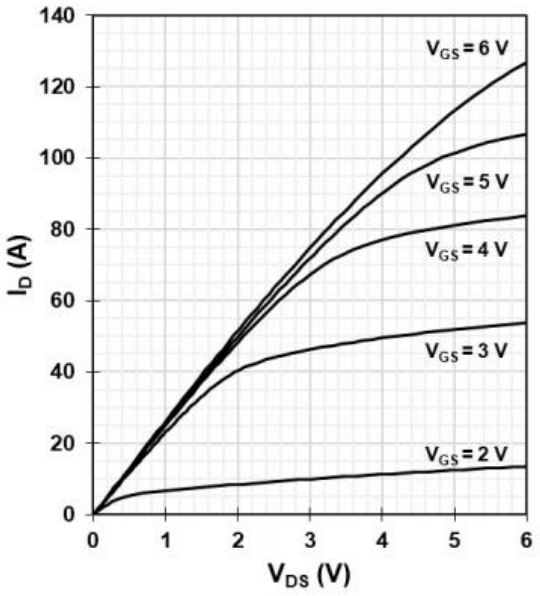
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Gate Threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=8mA	1.2	1.7	2.6	V
		V_{DS}=V_{GS}, I_D=8mA,T_J=150°C		1.9		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V		2	50	µA
		V_{DS}=650V,V_{GS}=0V,T_J=150°C		20		µA
Gate-source leakage current	I_{GSS}	V_{GS}=6V, V_{DS}=0V		170		µA
Static Drain to Source on resistance	$R_{DS(on)}$	V_{GS}= 6V, I_D=9A		42	55	mΩ
		V_{GS}= 6V, I_D=9A,T_J=150°C		105		mΩ
Internal Gate Resistance	R_G	f = 5 MHz; open drain		1.6		Ω
Dynamic Characteristics						
Input Capacitance	Ciss	V_{DS}=400V,V_{GS}=0V, f=1MHz		227		pF

Output Capacitance	Coss			60		pF
Reverse transfer capacitance	Crss			0.8		pF
Effective output capacitance, energy related[1]	$C_{O(er)}$	V_{DS}=0V to 400V,V_{GS}=0V		102		pF
Effective output capacitance, time related[2]	$C_{O(tr)}$			151		pF
Output charge	Q_{oss}	V_{DS}=0V to 400V,V_{GS}=0V,f=1MHz		60		nC
Output Capacitance Stored Energy	E_{oss}			8.2		μJ
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=400V,I_D=15A,L=90μH, V_{GS}=6V,R_{ON}=10Ω,R_{OFF}=1Ω		8.5		nS
Turn-Off Delay Time	$t_{d(off)}$			10.7		nS
Turn-On Rise Time	t_r			6.4		nS
Turn-Off Fall Time	t_f			5.9		nS
Switching Energy during turn-on	E_{on}			48		μJ
Switching Energy during turn-off	E_{off}			7.8		μJ
Gate charge Characteristics						
Gate charge	Q_G	V_{GS}=0 to 6V,V_{DS}=400V,I_D=30A		6.3		nC
Gate-source charge	Q_{GS}			1.6		nC
Gate-drain charge	Q_{GD}			1.9		nC
Gate plateau voltage	V_{plat}	V_{DS}=400V,I_D=30A		2.9		V
Reverse conduction Characteristics						
Source-drain reverse voltage	V_{SD}	V_{GS}=0V, I_{SD}=15A		2.9		V
Pulsed current, reverse	$I_{S,pulse}$	V_{GS}=6V		50		A
Reverse recovery charge [3]	Q_{rr}	I_{SD}=15A,V_{DS}=400V		0		nC
Reverse recovery time	t_{rr}			0		ns
Peak reverse recovery current	I_{rrm}			0		A

1. Co(er) is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. Co(tr) is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V
3. Excluding Q_{OSS}

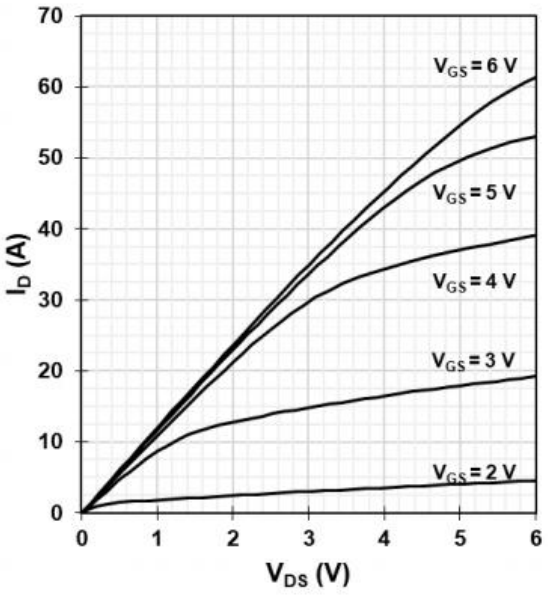
Electrical Characteristics Diagrams(at T_J=25℃,unless otherwise specified.)

Figure 1 Typ. output characteristics



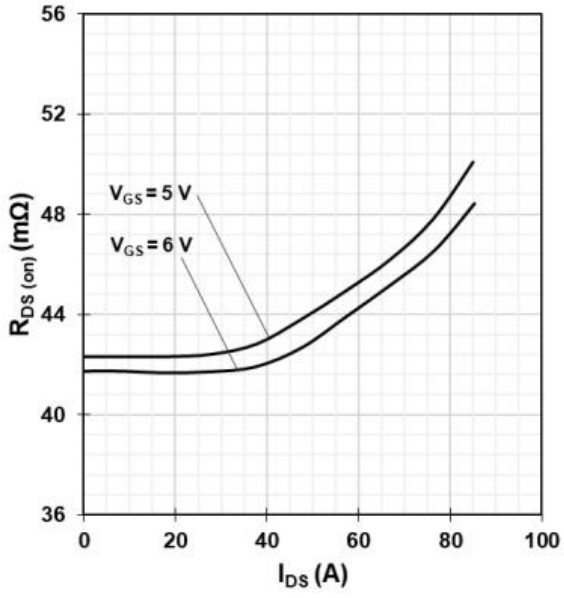
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



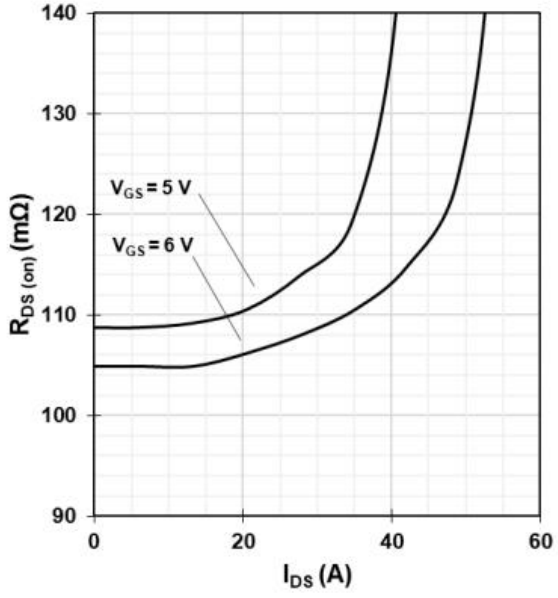
$I_D = f(V_{DS}, V_{GS})$; T_j = 150 °C

Figure 3 Typ. drain-source on-state resistance



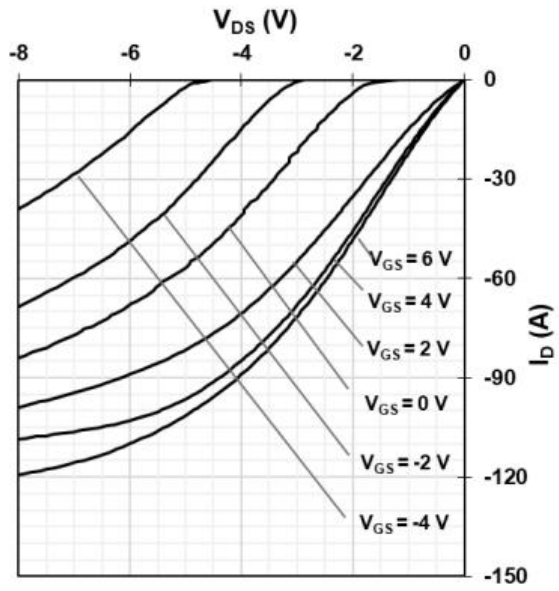
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



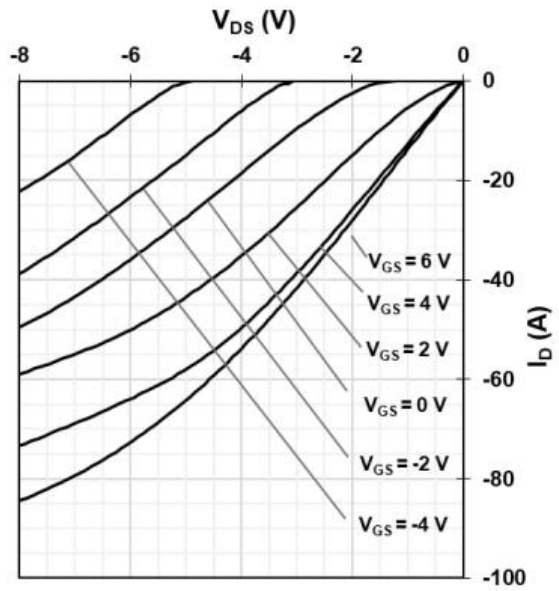
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 150 °C

Figure 5 Typ. channel reverse characteristics



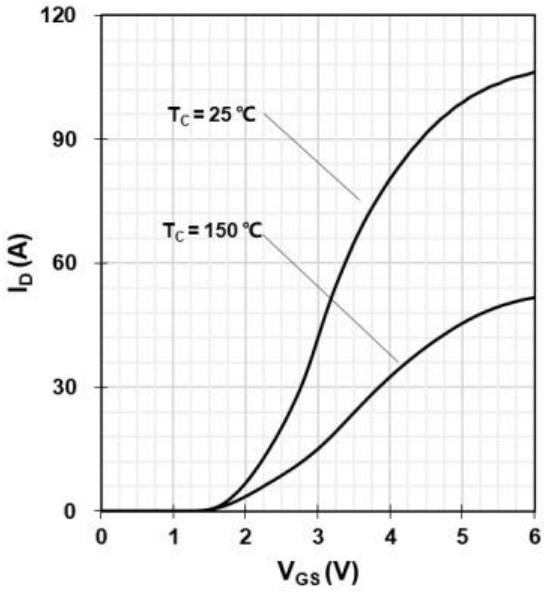
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



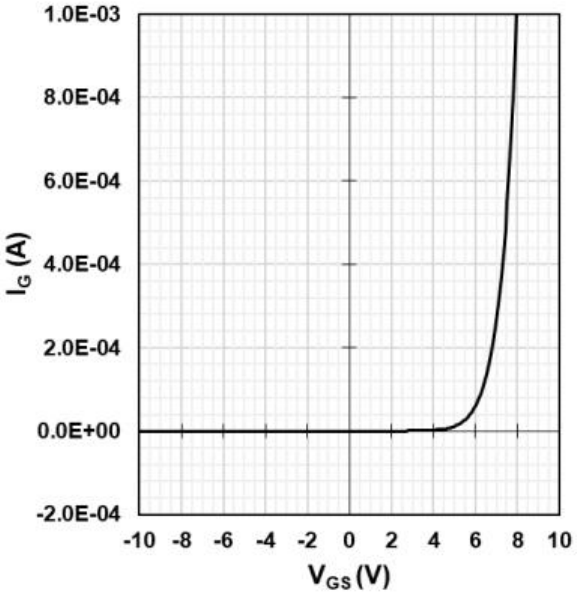
$I_D = f(V_{DS}, V_{GS})$; T_j = 150 °C

Figure 7 Typ. transfer characteristics



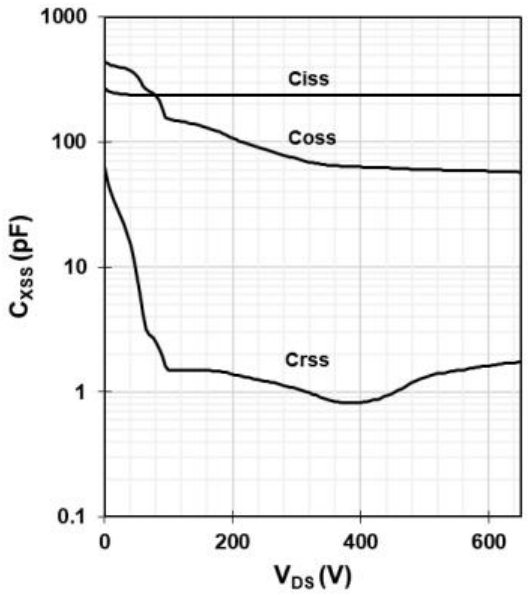
$I_D = f(V_{GS})$; V_{DS} = 5 V

Figure 8 Typ. gate-to-source leakage



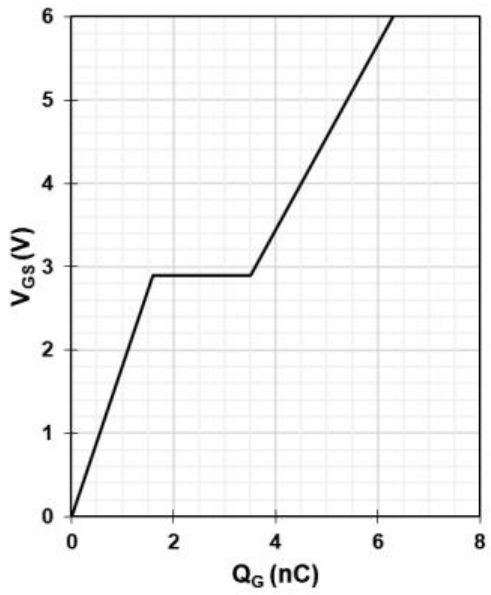
$I_G = f(V_{GS})$; V_D = open

Figure 9 Typ. capacitances



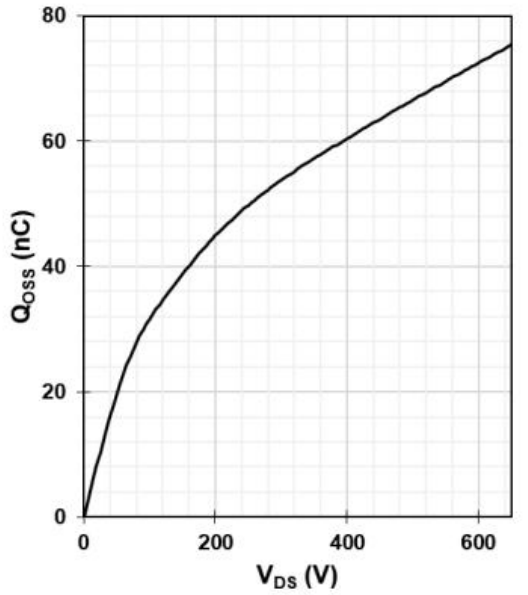
C_{XSS} = f(V_{DS}); Freq. = 1 MHz

Figure 10 Typ. gate charge



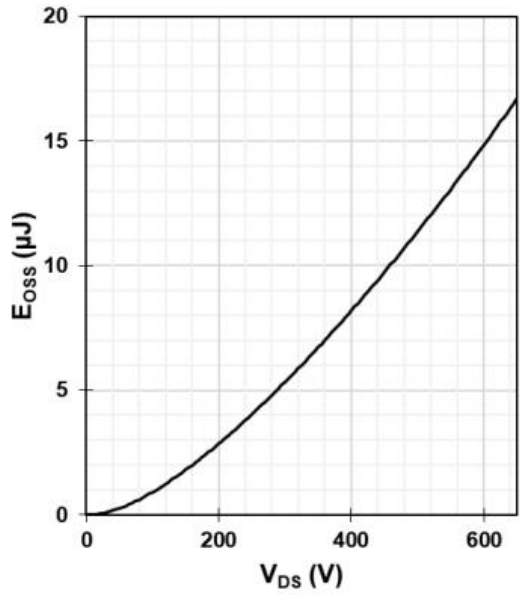
V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 30 A

Figure 11 Typ. output charge



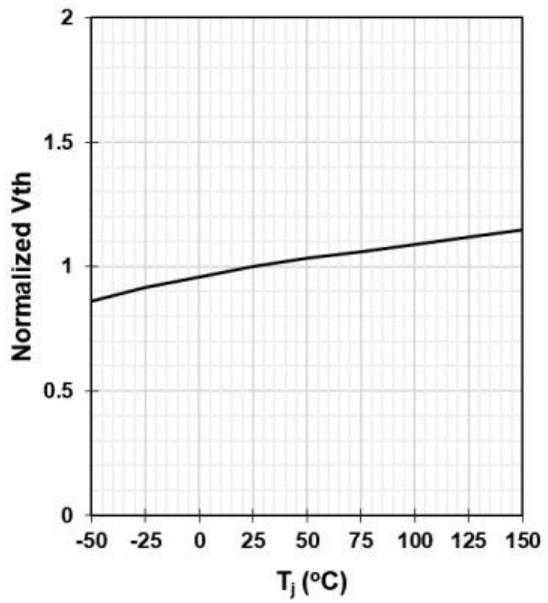
Q_{OSS} = f(V_{DS}); Freq. = 1 MHz

Figure 12 Typ. C_{OSS} stored energy



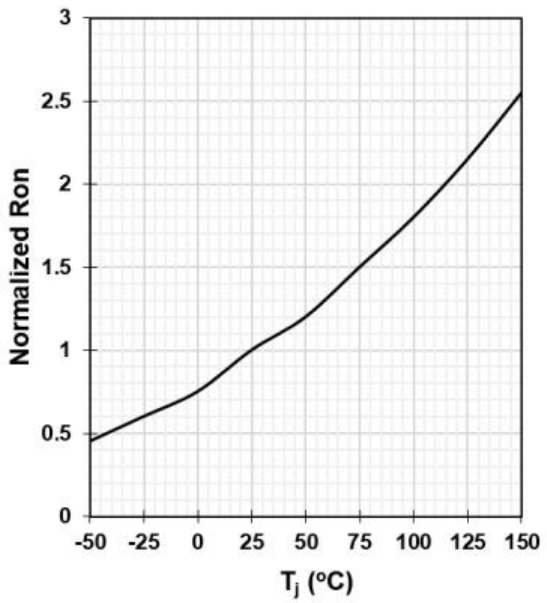
E_{OSS} = f(V_{DS}); Freq. = 1 MHz

Figure 13 Gate threshold voltage



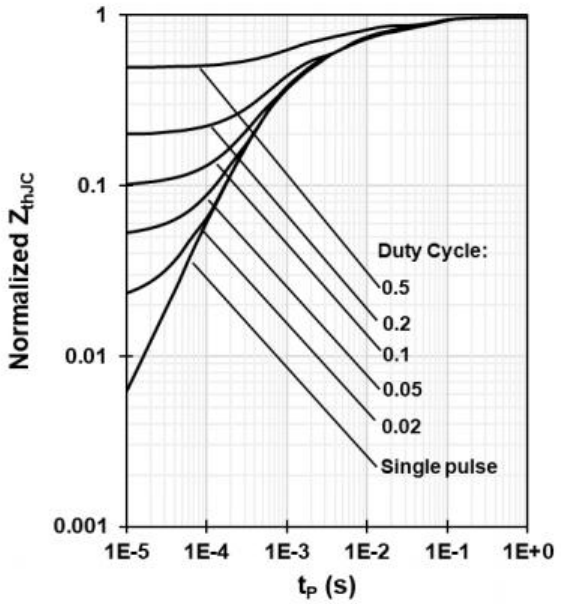
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 7.3$ mA

Figure 14 Drain-source on-state resistance



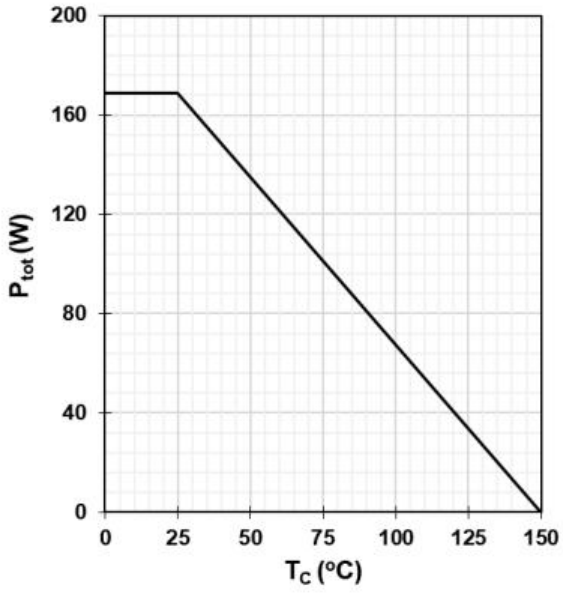
$R_{DS(on)} = f(T_j)$; $I_D = 5.3$ A; $V_{GS} = 6$ V

Figure 15 Max. transient thermal impedance



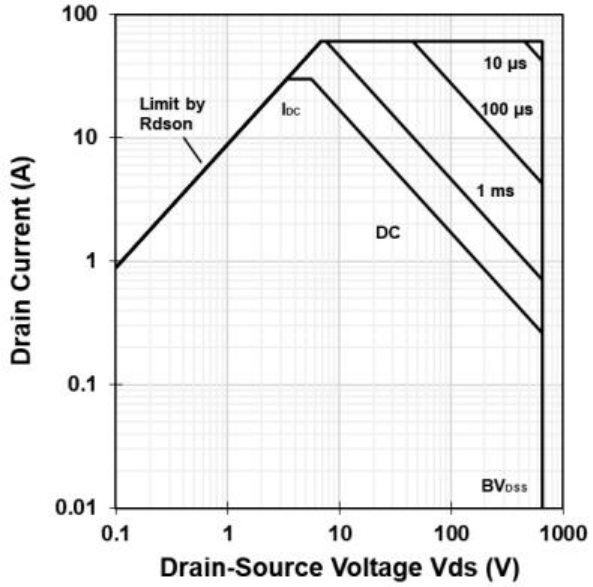
$Z_{thJC} = f(t_P, D)$

Figure 16 Power dissipation



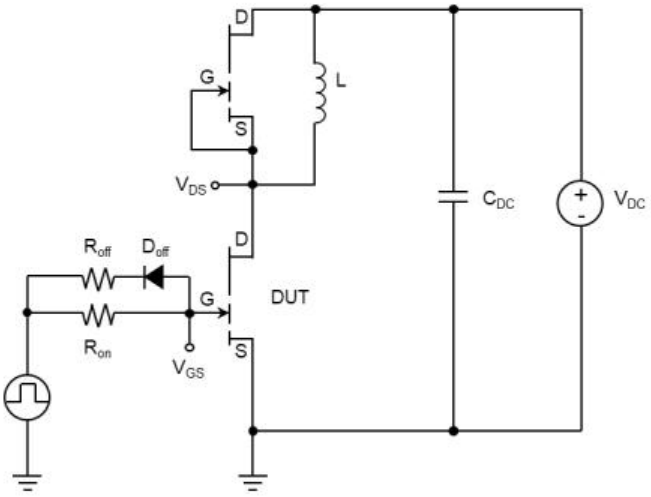
$P_{tot} = f(T_C)$

Figure 17 Safe operating area



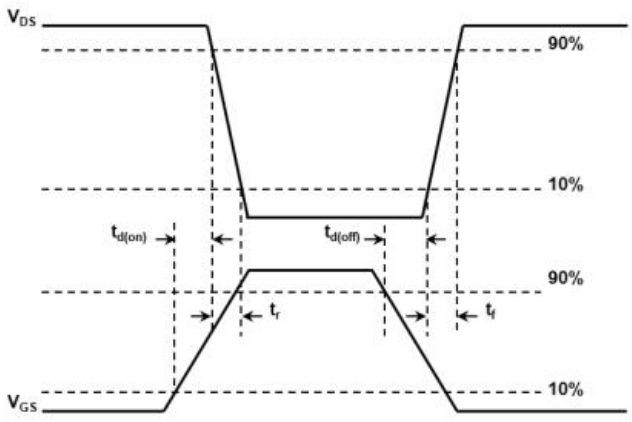
$I_D = f(V_{DS})$; $T_C = 25$ °C

Figure 18 Switching time test circuit



V_{DS} = 400 V, I_D = 15 A, L = 90 µH, V_{GS} = 6 V,
R_{on} = 10 Ω, R_{off} = 1 Ω

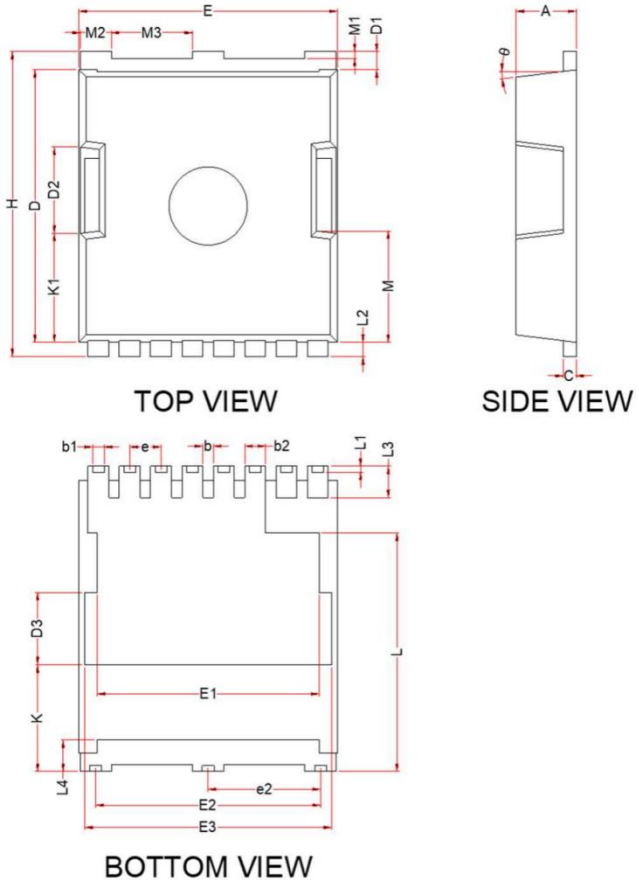
Figure 19 Typ. switching time waveform



Package Information

TOLL

Dimensions in mm



SYMBOL	MIN	MAX
A	2.20	2.40
b	0.30	0.50
b1	0.35	0.55
b2	0.70	0.90
c	0.40	0.60
D	10.28	10.58
D1	0.60	0.80
D2	(3.30)	
D3	(2.77)	
E	9.70	10.10
E1	(8.50)	
E2	(8.50)	
E3	(9.46)	
e	1.10	1.30
H	11.48	11.88
K	(4.08)	
K1	(4.17)	
L	(9.13)	
L1	0.13	0.33
L2	0.50	0.70
L3	1.10	1.30
L4	1.10	1.30
M	(4.23)	
M1	0.16	0.36
M2	1.10	1.30
M3	3.00	3.20
θ	4°	10°
e2	4.20	4.40

Tape and reel information