



SKGM18N65-N8

Enhancement-mode GaN Power Transistor

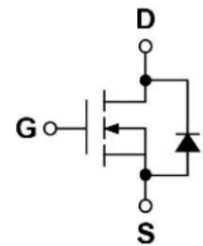
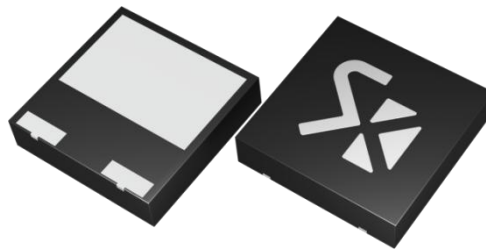
Features

- Easy to use, compatible with standard gate driver
- Excellent $Q_G \cdot R_{DS(on)}$ figure of merit(FOM)
- Low Q_{RR} , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Key Performance Parameters at $T_J=25^\circ\text{C}$		
Parameters	Values	Units
$V_{DS,max}$	650	V
$R_{DS(on),max}$	150	$m\Omega$
$Q_{G,typ}$	11.5	nC
$I_{D,Pulse}$	17	A
Q_{RR}	66	nC

Applications

- Power adapters
- Telecom and datacom
- Automotive
- Servo motors



Description

650V GaN-On-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead Package (DFN) with 8 mm *8 mm Size.

Package Marking and Ordering Information

Part Number	Package	Packaging	Base QTY
SKGM18N65-N8	DFN 8 x 8	Tape and Reel	2500

Absolute Maximum Ratings(at $T_J = 25^\circ\text{C}$ unless otherwise specified.)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Drain-source voltage		$V_{DS,max}$	$T_J = -55^\circ\text{C}$ to 150°C			650	V
Drain-source voltage transient ¹		$V_{DS,transient}$	$V_{GS}=0V, V_{DS}=800V$			800	V
Continuous current, drain-source		I_D	$T_C=25^\circ\text{C}$			17	A
			$T_C=100^\circ\text{C}$			10.6	A
Pulsed current, drain-source		$I_{D,pulse}$	$T_C=25^\circ\text{C}; (\text{pulse width: } 10\mu\text{s})$			64	A
Pulsed current, drain-source		$I_{D,pulse}$	$T_C=150^\circ\text{C}; (\text{pulse width: } 10\mu\text{s})$			47	A
Gate-source voltage, continuous		V_{GS}		-20		+20	V
Power dissipation		P_D	$T_C=25^\circ\text{C}$			67.5	W
Operating temperature	Case	T_C		-55		150	$^\circ\text{C}$
	Junction	T_J		-55		150	$^\circ\text{C}$
Storage temperature		T_{STG}		-55		150	$^\circ\text{C}$

1. Off-state spike duty cycle < 0.01, spike duration < 2 μs



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Thermal Characteristics

Parameter	Symbol	Notes/Test Condition	Values			Unit
			Min	Typ	Max	
Thermal Resistance, Junction to Case	$R_{\theta JC}$				1.85	°C/W
Thermal Resistance, Junction to ambient ¹	$R_{\theta JA}$				50	°C/W
Reflow soldering temperature	T_{SOLD}				260	°C

1. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70 μ m thickness).

Electrical Characteristics (at $T_J = 25^\circ\text{C}$, unless specified otherwise.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Gate Threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =500μA	3	4	5	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =700V, V _{GS} =0V,T _J =25°C		8	20	μA
		V _{DS} =700V,V _{GS} =0V,T _J =125°C		50		μA
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±150	μA
Static Drain to Source on resistance ¹	R _{DS(on)}	V _{GS} =12V, I _D =4A,T _J =25°C		120	150	mΩ
		V _{GS} =12V, I _D =4A,T _J =125°C		240		mΩ
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} =400V,V _{GS} =0V, f=100kHz		604		pF
Output Capacitance	C _{oss}			58		pF
Reverse transfer capacitance	C _{rss}			1.2		pF
Effective output capacitance,energy related	C _{O(er)}	V _{DS} =0V to 400V,V _{GS} =0V		84		pF
Effective output capacitance,time related	C _{O(tr)}			165		pF
Output charge	Q _{OSS}	V _{DS} =0V to 400V,V _{GS} =0V		66		nC
Turn-On Delay Time	t _{d(on)}	V _{DS} =400V,I _D =10A, V _{GS} =0~12V,R _G =40Ω		44		nS
Turn-Off Delay Time	t _{d(off)}			40		nS
Turn-On Rise Time	t _r			16		nS
Turn-Off Fall Time	t _f			12		nS
Gate charge characteristics						
Gate charge	Q _G	V _{DS} =400V,I _D =6A, V _{GS} =0~12V		11.5		nC
Gate-source charge	Q _{GS}			4		nC



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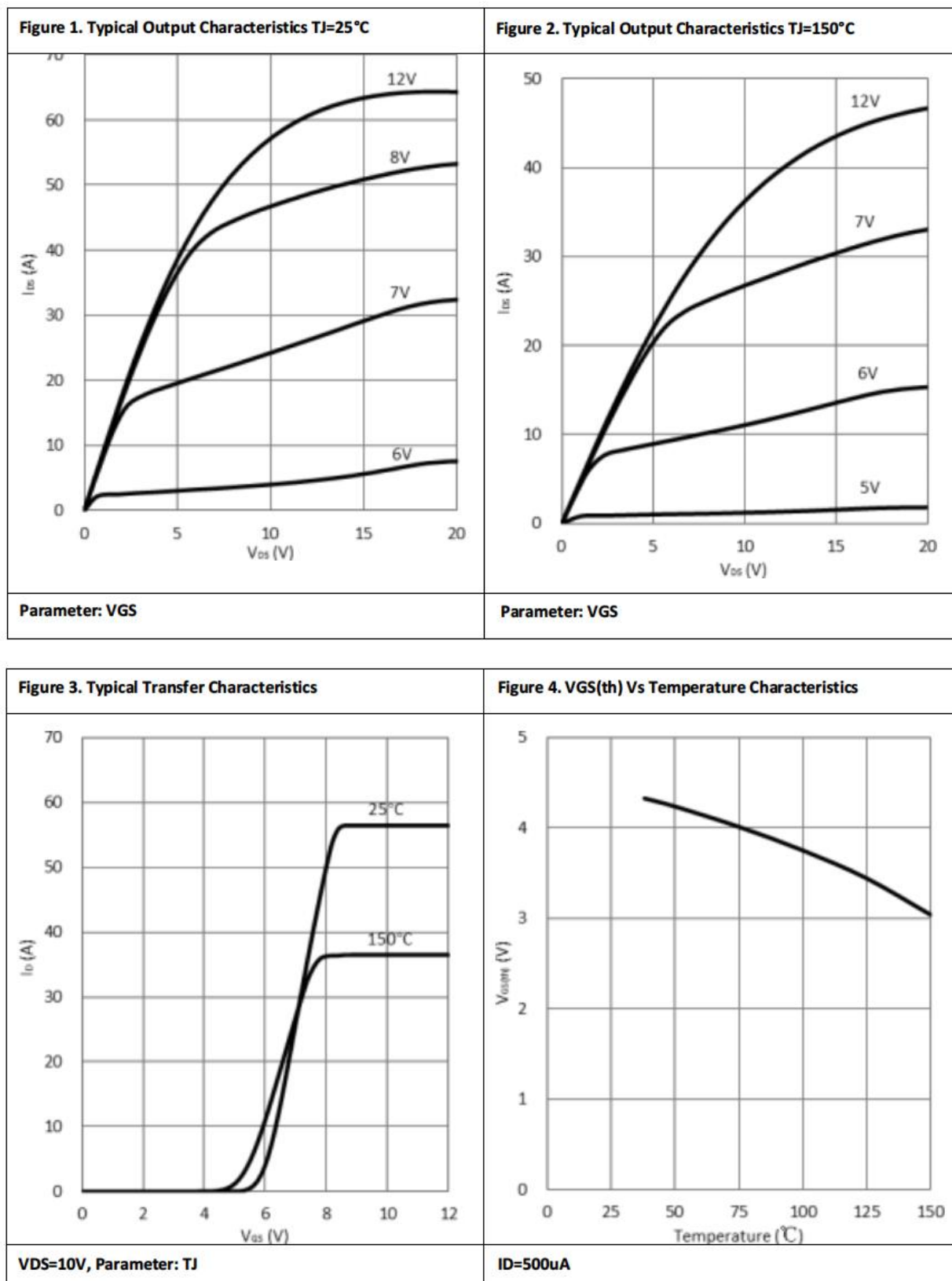
Gate-drain charge	Q_{GD}			3		nC
Reverse conduction characteristics						
Source-drain reverse voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}, T_J = 25^\circ\text{C}$		1.3		V
		$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}, T_J = 25^\circ\text{C}$		1.8		V
		$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}, T_J = 150^\circ\text{C}$		2.6		V
Reverse recovery time	t_{rr}	$I_{SD} = 10\text{ A}, V_{GS} = 0\text{ V},$ $di/dt = 1000\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$		27		ns
Reverse recovery charge	Q_{RR}			66		nC

1. Dynamic on-resistance; see Figure 17 and 18 for test circuit and configurations.



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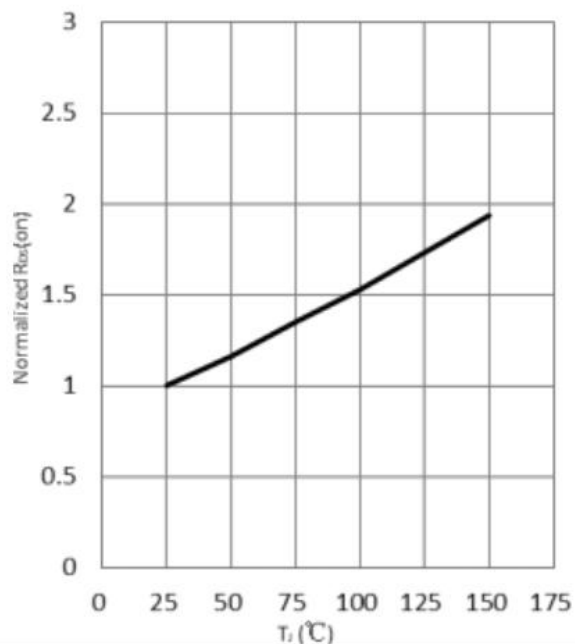
Electrical Characteristics Diagrams(at $T_J = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.)





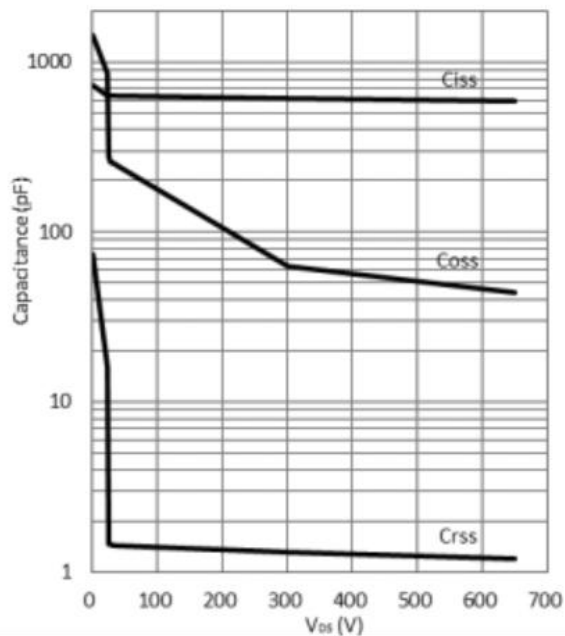
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Figure 5. Normalized On-resistance



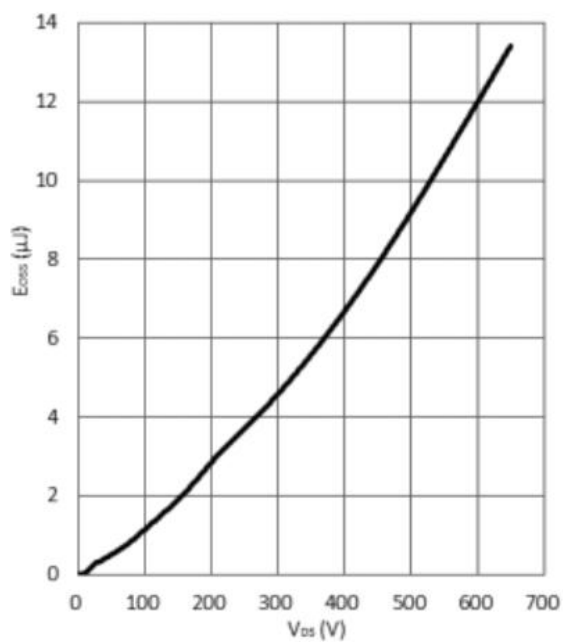
$I_D=4\text{A}, V_{GS}=12\text{V}$

Figure 6. Typical Capacitance



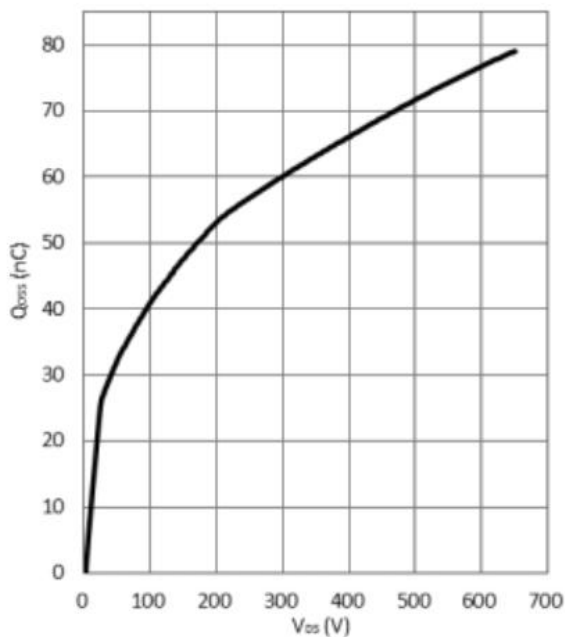
$V_{GS}=0\text{V}, f=1\text{MHz}$

Figure 7. Typical C_{oss} Stored Energy



$V_{GS}=0\text{V}, f=1\text{MHz}$

Figure 8. Typical Q_{oss}

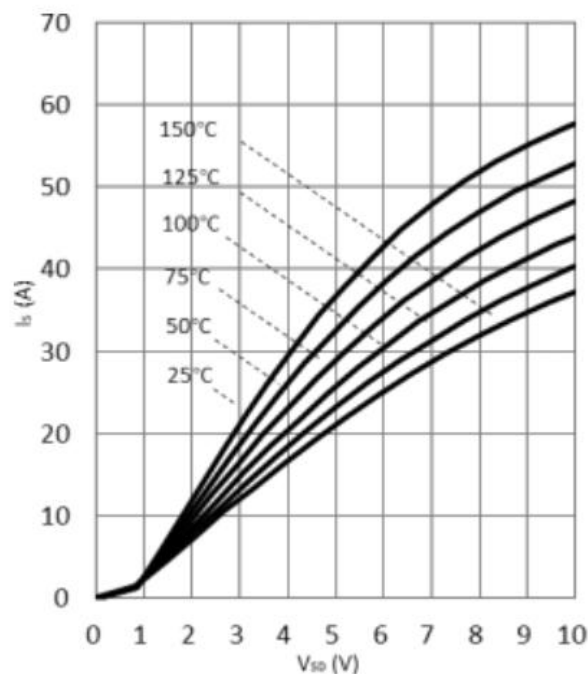


$V_{GS}=0\text{V}, f=1\text{MHz}$



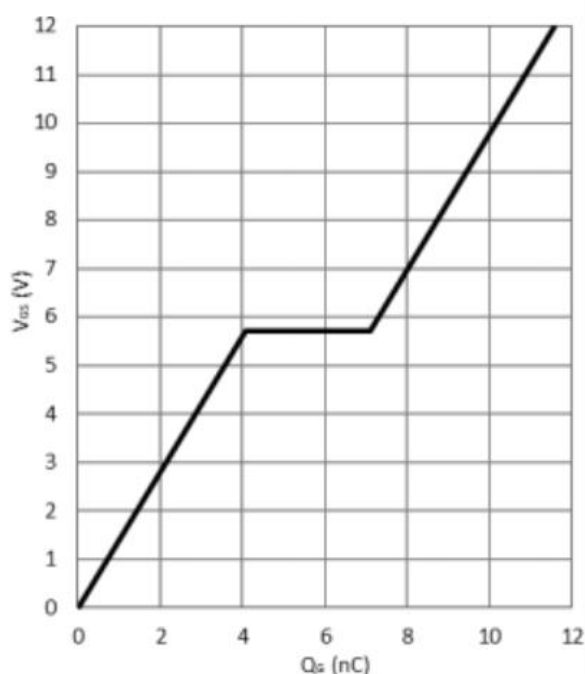
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Figure 9. Forward Characteristic of Rev. Diode



$I_s = f(V_{SD}), \text{Parameter } T_J$

Figure 10. Typical Gate Charge



$I_D = 6A, V_{DS} = 400V$

Figure 11. Power Dissipation

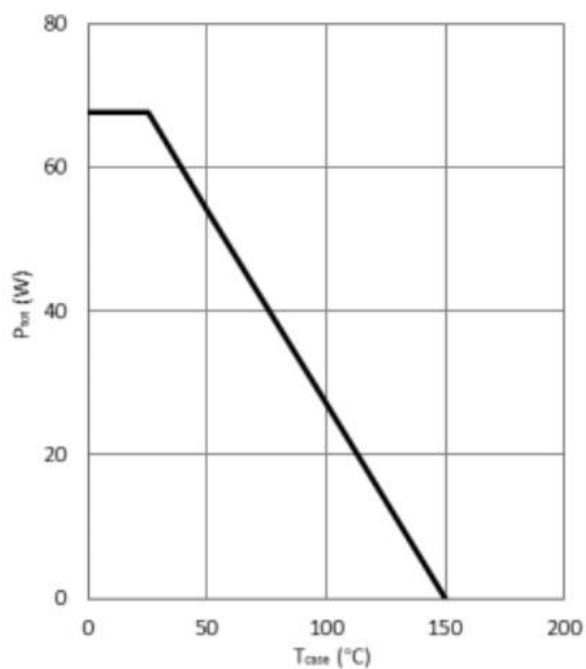
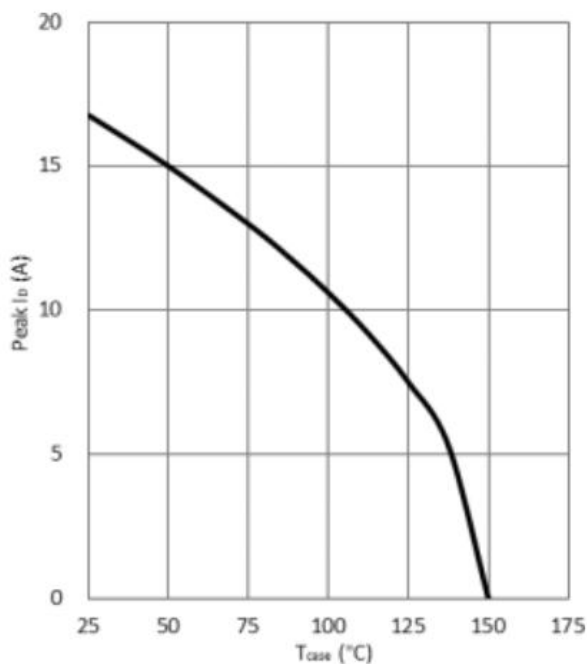


Figure 12. Current Derating





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Figure 13. Transient Thermal Resistance

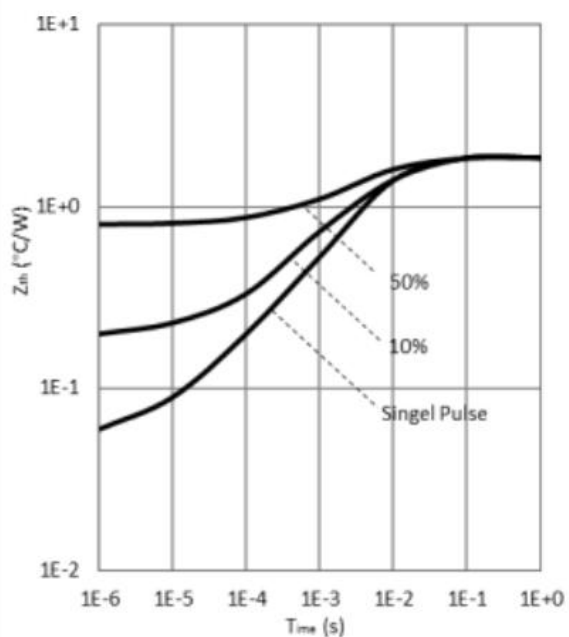
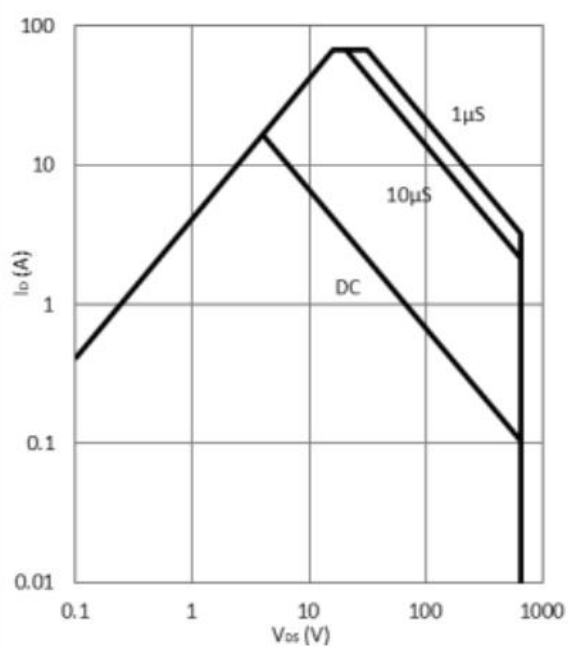
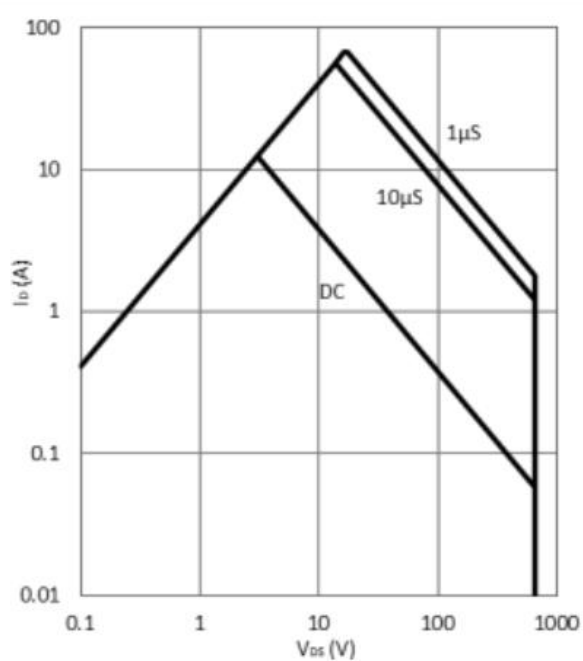


Figure 14. Safe Operating Area TC=25°C



calculated based on thermal limit

Figure 15. Safe Operating Area TC=80°C





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Figure 17. Switching Time Test Circuit

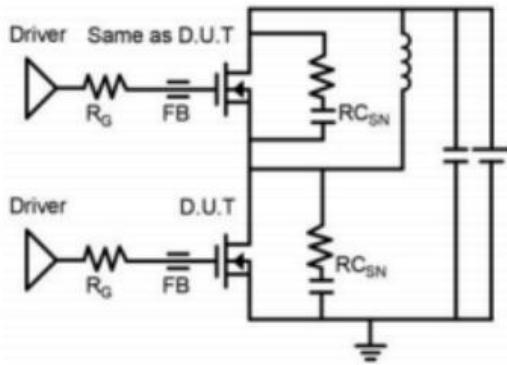


Figure 18. Switching Time Waveform

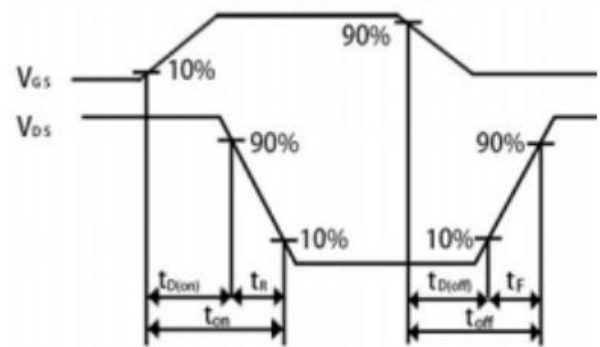


Figure 19. Dynamic R_{DS(on)} Test Circuit

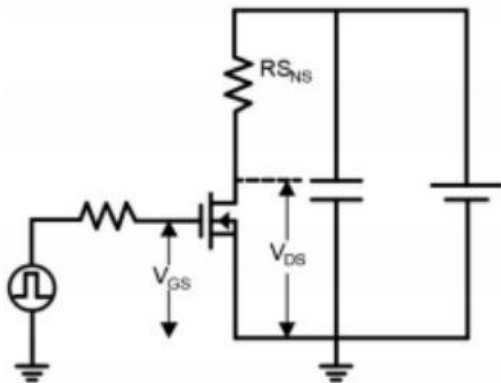


Figure 20. Dynamic R_{DS(on)} Waveform

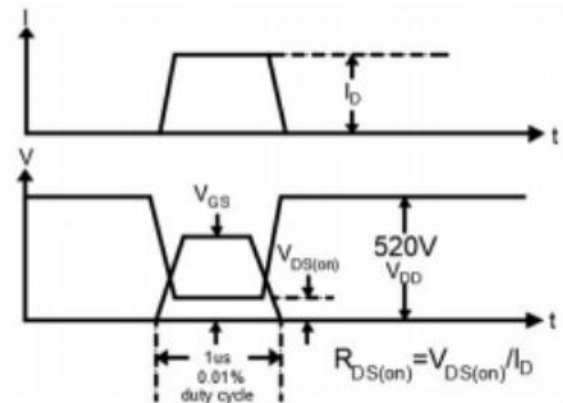


Figure 21. Diode Characteristic Test Circuits

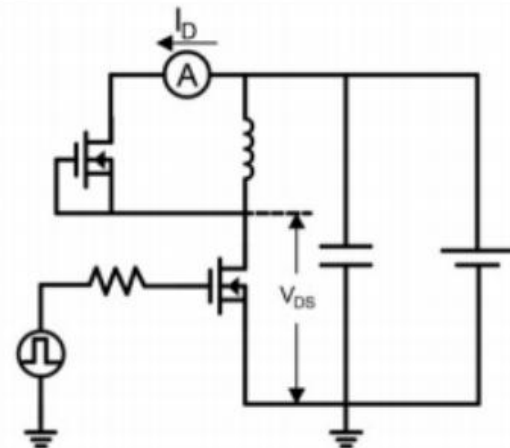
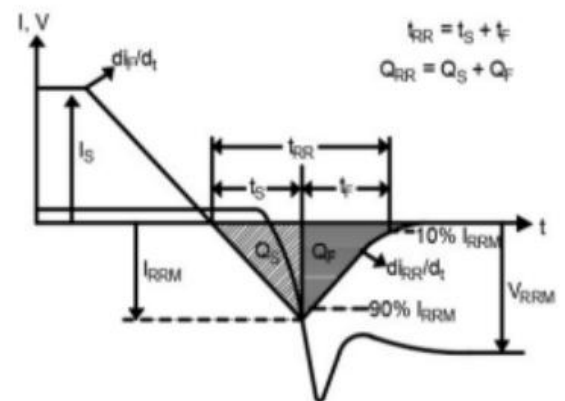


Figure 22. Diode Recovery Waveform



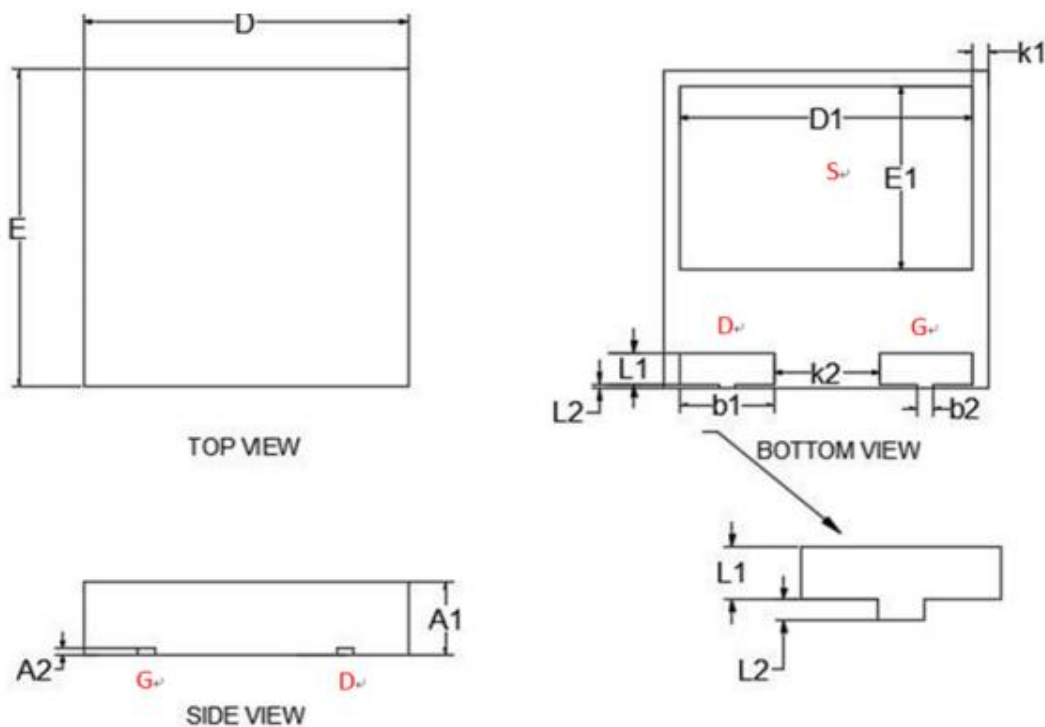


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Package Information

DFN8*8

Dimensions in mm

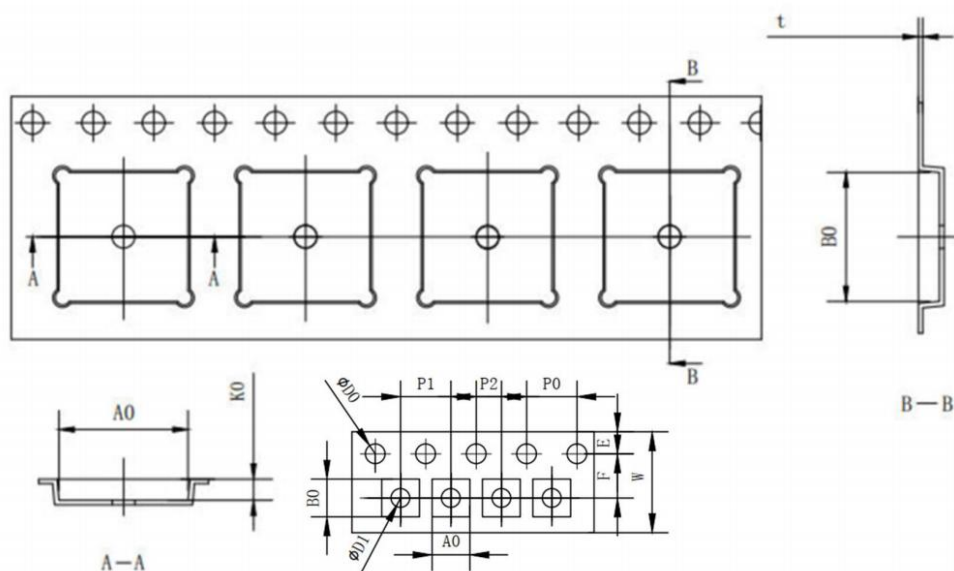


Symbol	Millimeter		
	Min	Nom	Max
A1	0.80	0.90	1.15
A2	0.19	0.203	0.22
b1	2.20	2.30	2.40
b2	0.80REF		
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D1	6.90	7.20	7.50
E1	4.40	4.60	4.80
L1	0.70	0.80	0.90
L2	0.12REF		
K1	0.30	0.40	0.50
K2	2.50	2.60	2.70
F	2.05	2.15	2.35



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Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	t	0.30±0.05
P2	2.00±0.10		

