



SKGM17N65AD8

Enhancement-mode GaN Power Transistor

Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High-density power conversion
- High-efficiency power conversion

Description

650V GaN-On-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead Package (DFN) with 5 mm *6 mm Size.

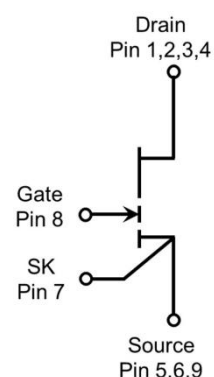
Ordering Information

Type/Ordering Code	Package	Marking
	DFN 5x6 2500 pcs/reel	

Absolute Maximum Ratings(at $T_J = 25^{\circ}\text{C}$ unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-source voltage	$V_{DS,max}$	$V_{GS}=0V, I_D=10\mu A$			650	V
Drain-source voltage transient ¹	$V_{DS,transient}$	$V_{GS}=0V, V_{DS}=750V$			750	V
Continuous current, drain-source	I_D	$T_C=25^{\circ}\text{C}$			17	A
Pulsed current, drain-source ²	$I_{D,pulse}$	$T_C=25^{\circ}\text{C}; V_G=6V$			32	A
Pulsed current, drain-source ²	$I_{D,pulse}$	$T_C=125^{\circ}\text{C}; V_G=6V$			18	A
Gate-source voltage, continuous ³	V_{GS}	$T_J = -55^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	-1.4		+7	V
Gate-source voltage, pulsed	$V_{GS,pulse}$	$T_J = -55^{\circ}\text{C} \text{ to } 150^{\circ}\text{C};$			+10	V

Key Performance Parameters at $T_J=25^{\circ}\text{C}$		
Parameters	Values	Units
$V_{DS,max}$	650	V
$R_{DS(on),max}$	140	m Ω
$Q_{G,typ}$	3.3	nC
$I_{D,Pulse}$	32	A
$Q_{OSS,@400V}$	33	nC
Q_{rr}	0	nC



Gate	8
Drain	1, 2, 3, 4
Kelvin Source	7
Source	5, 6, 9



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		$t_{\text{pluse}}=50\text{ns}, f=100\text{kHz}; \text{Open drain}$				
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$			113	W
Operating temperature	T_J		-55		150	$^\circ\text{C}$
Storage temperature	T_{STG}		-55		150	$^\circ\text{C}$

1. V_{DS} , transient is intended for surge rating during non-repetitive events, $t_{\text{pulse}} < 1 \mu\text{s}$.
2. Pulse width = $10\mu\text{s}$.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

Thermal Characteristics

Parameter	Symbol	Notes/Test Conditions	Value	Unit
Thermal Resistance, Junction to Case, Max.	$R_{\theta\text{JC}}$		1.1	$^\circ\text{C}/\text{W}$
Reflow soldering temperature, Max.	T_{SOLD}	MSL3	260	$^\circ\text{C}$

Electrical Characteristics(at $T_J = 25^\circ\text{C}$, unless specified otherwise.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Gate Threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=17.2\text{mA}, T_J=25^\circ\text{C}$	1.2	1.7	2.5	V
		$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=17.2\text{mA}, T_J=125^\circ\text{C}$		1.6		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}, T_J=25^\circ\text{C}$		0.6	20	μA
		$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}, T_J=125^\circ\text{C}$		1		μA
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=6\text{V}, V_{\text{DS}}=0\text{V}$		40	200	μA
Static Drain to Source on resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=6\text{V}, I_{\text{D}}=5\text{A}, T_J=25^\circ\text{C}$		100	140	$\text{m}\Omega$
		$V_{\text{GS}}=6\text{V}, I_{\text{D}}=5\text{A}, T_J=125^\circ\text{C}$		200		$\text{m}\Omega$
Internal Gate Resistance	R_{G}	$f=5\text{MHz}, \text{open drain}$		3.5		Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}}=400\text{V}, V_{\text{GS}}=0\text{V}, f=100\text{kHz}$		125		pF
Output Capacitance	C_{oss}			40		pF
Reverse transfer capacitance	C_{rss}			0.5		pF
Effective output capacitance,energy related ¹	$C_{\text{O(er)}}$	$V_{\text{DS}}=0\text{V to } 400\text{V}, V_{\text{GS}}=0\text{V}$		53		pF
Effective output capacitance,time related ²	$C_{\text{O(tr)}}$			81		pF
Output charge	Q_{OSS}	$V_{\text{DS}}=0\text{V to } 400\text{V}, V_{\text{GS}}=0\text{V}$		33		nC
Gate charge characteristics						
Gate charge	Q_{G}	$V_{\text{GS}}=0\text{ to } 6\text{V}, V_{\text{DS}}=400\text{V}, I_{\text{D}}=5\text{A}$		3.3		nC



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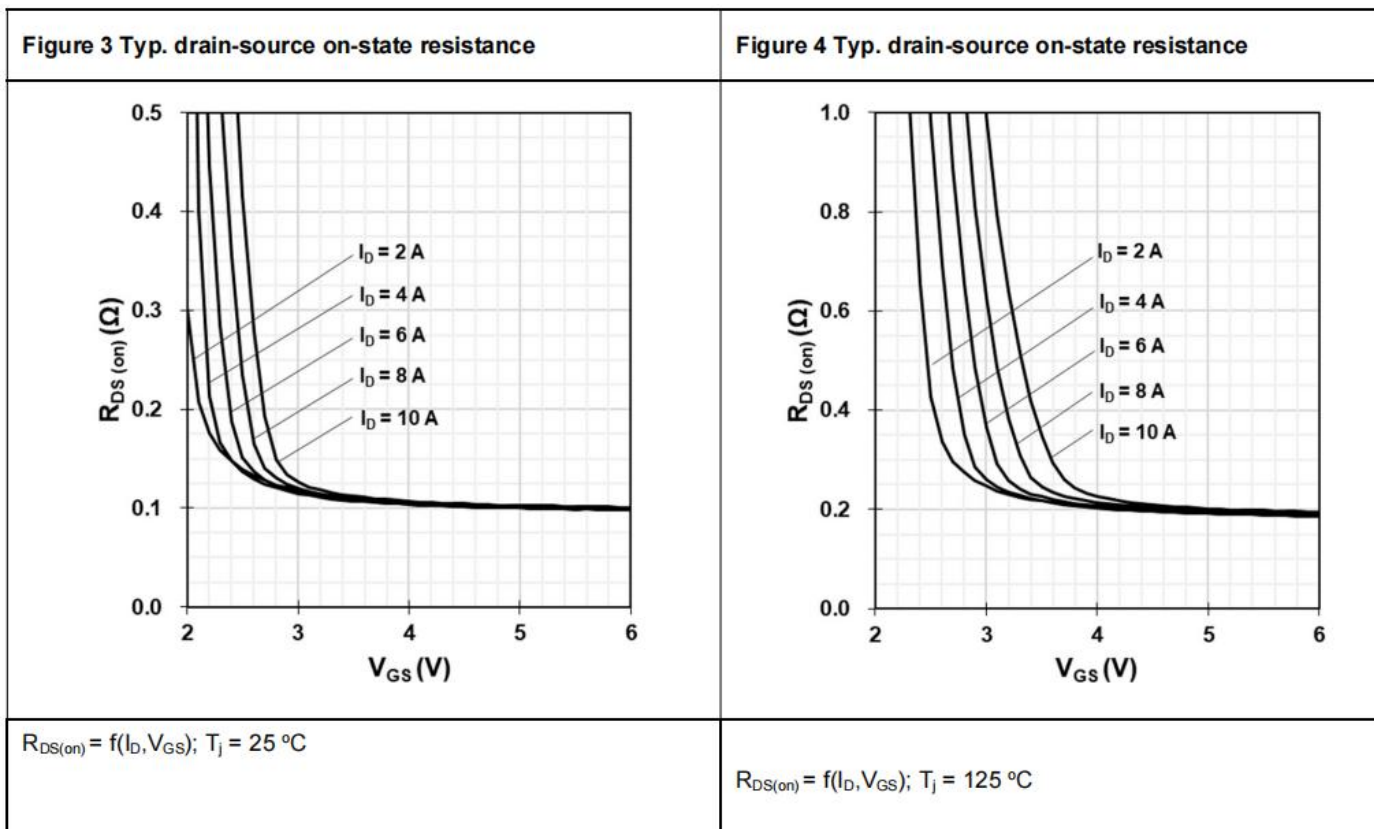
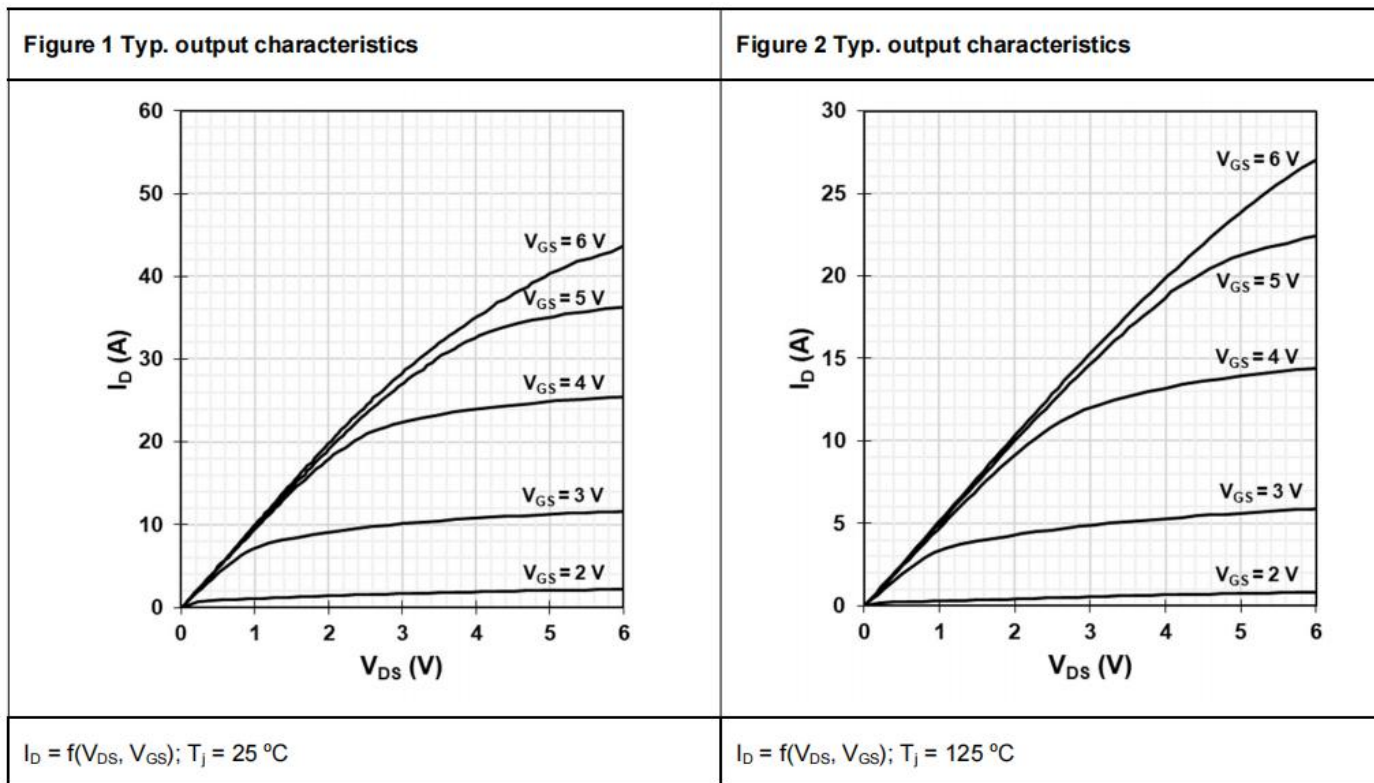
Gate-source charge	Q_{GS}			0.3		nC
Gate-drain charge	Q_{GD}			1.25		nC
Gate plateau voltage	V_{plat}	$V_{DS} = 400\text{ V}, I_D = 5\text{ A}$		2.4		nC
Reverse conduction characteristics						
Source-drain reverse voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$		2.5		V
Pulsed current, reverse	$I_{S,pulse}$	$V_{GS} = 6\text{ V}$		28		A
Reverse recovery charge	Q_{rr}	$I_{SD} = 5\text{ A}, V_{DS} = 400\text{ V}$		0		nC
Reverse recovery time	t_{rr}			0		ns
Peak reverse recovery current	I_{rrm}			0		A

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.



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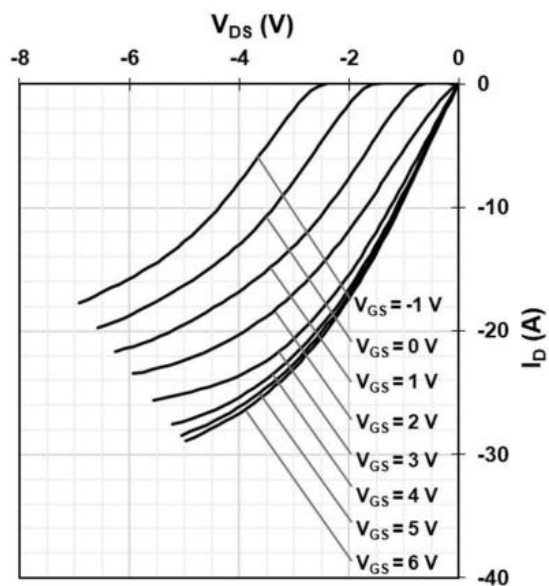
Electrical Characteristics Diagrams(at $T_J = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.)





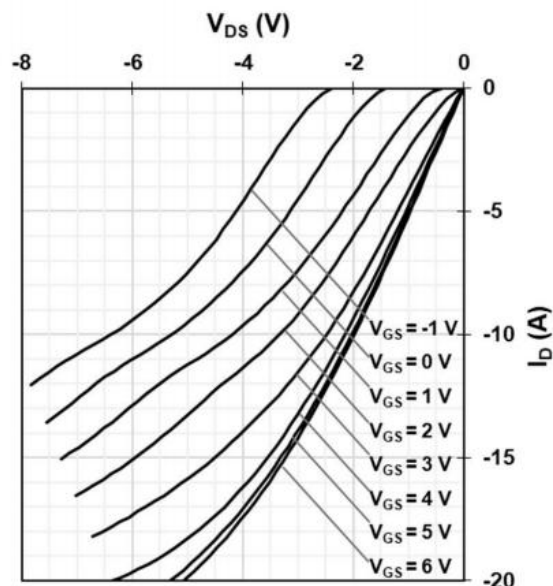
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Figure 5 Typ. channel reverse characteristics



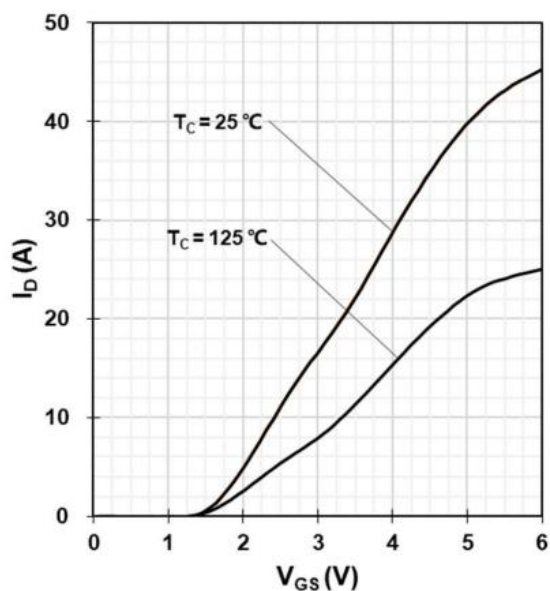
$$I_D = f(V_{DS}, V_{GS}); T_J = 25^\circ\text{C}$$

Figure 6 Typ. channel reverse characteristics



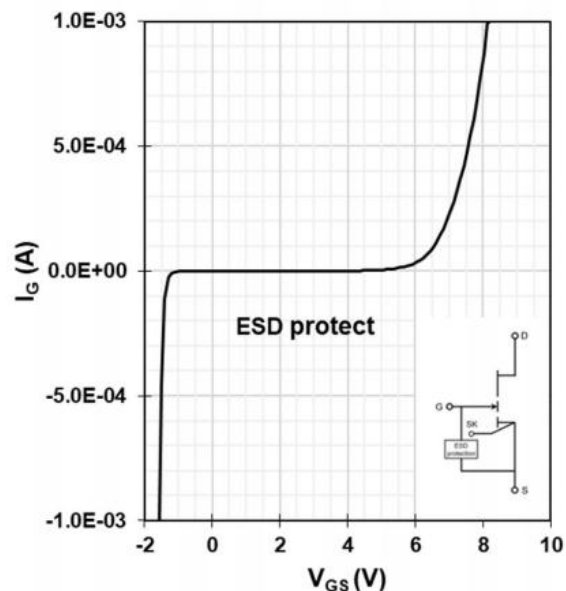
$$I_D = f(V_{DS}, V_{GS}); T_J = 125^\circ\text{C}$$

Figure 7 Typ. transfer characteristics



$$I_D = f(V_{GS}); V_{DS} = 5\text{ V}$$

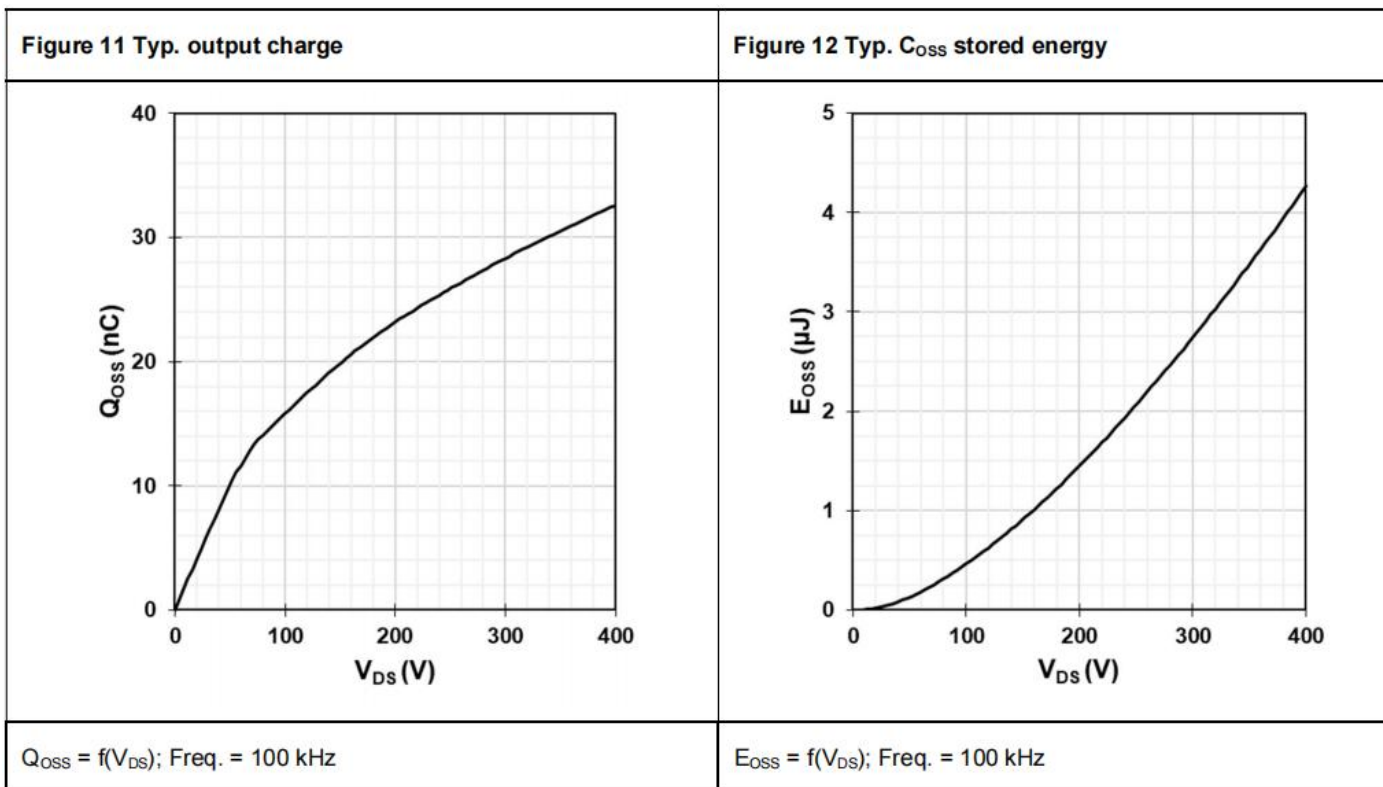
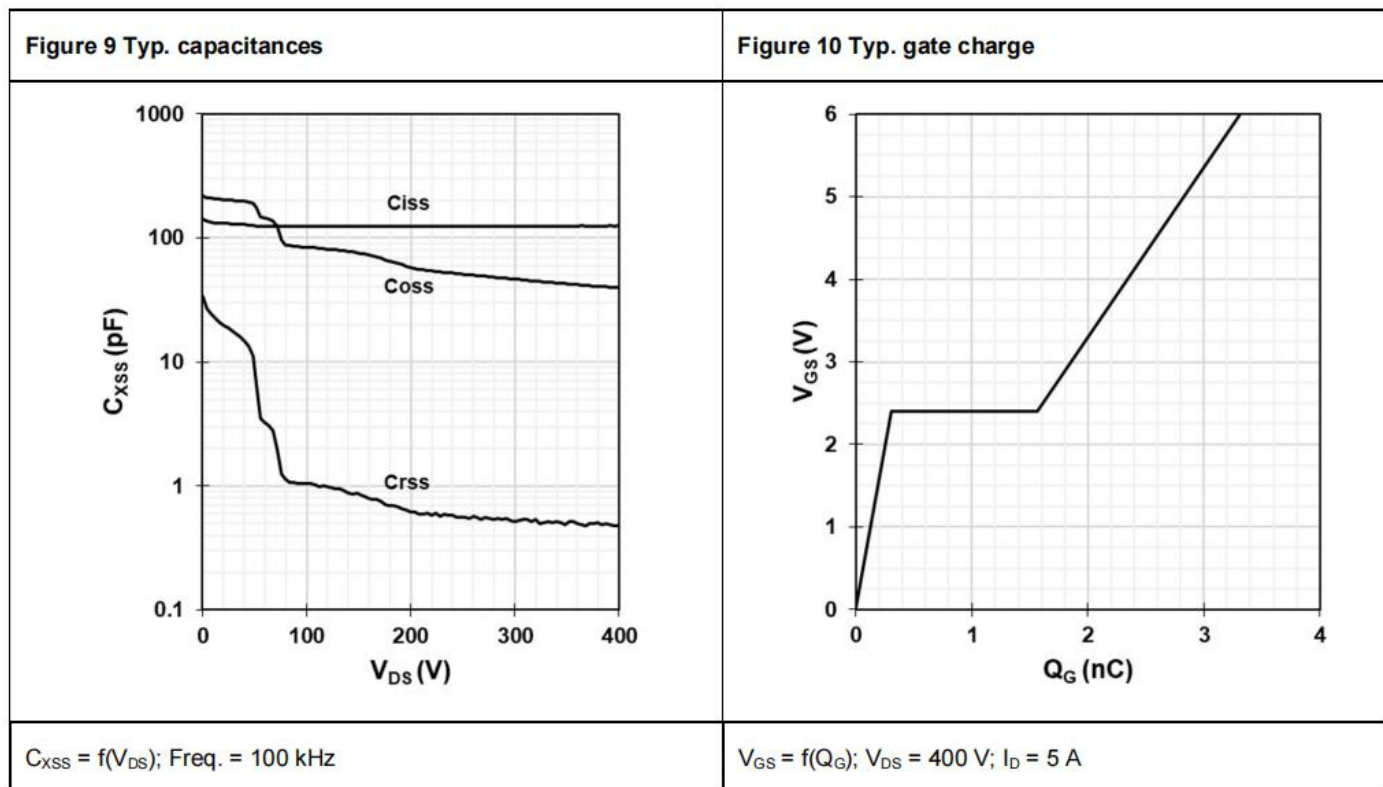
Figure 8 Typ. gate-to-source leakage



$$I_G = f(V_{GS}); I_G \text{ reverse turn on by ESD unit; } V_D = \text{open}$$



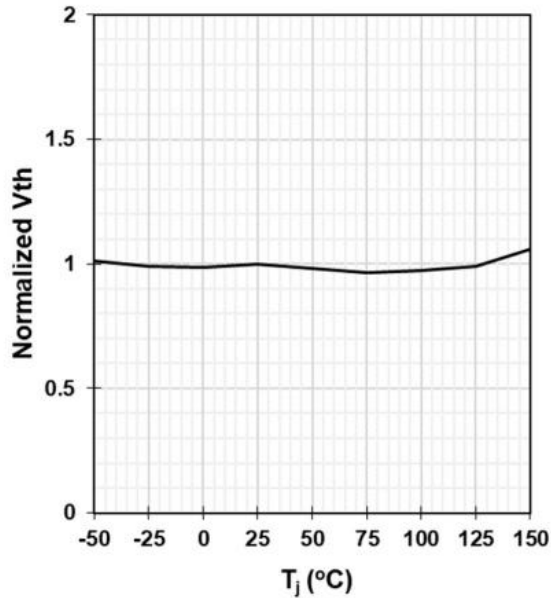
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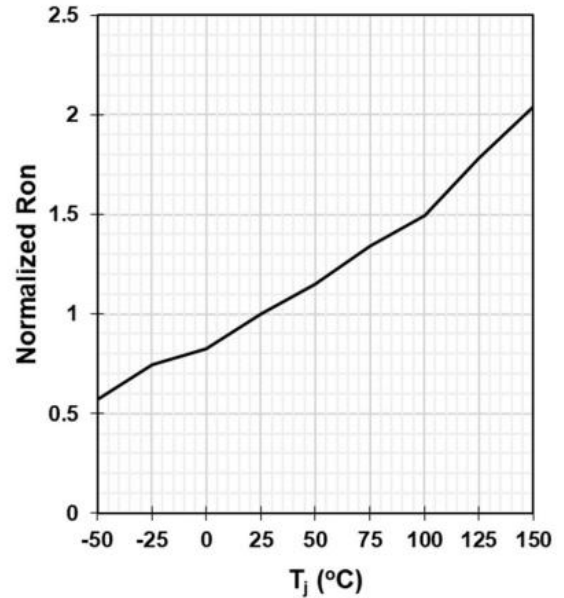
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Figure 13 Gate threshold voltage



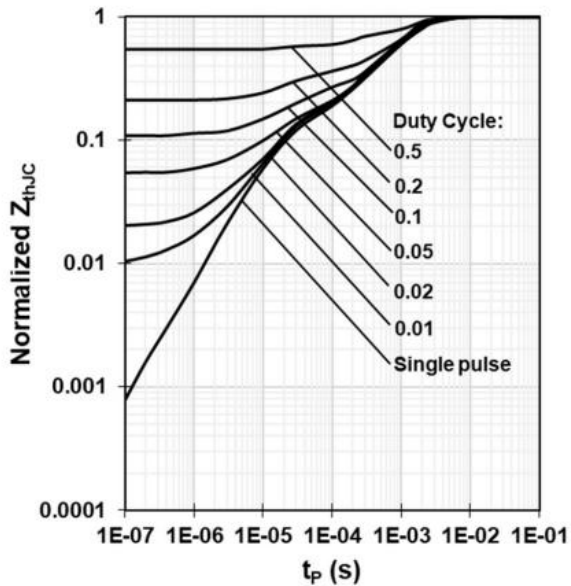
$$V_{GS(TH)} = f(T_j); V_{GS} = V_{DS}; I_D = 17.2 \text{ mA}$$

Figure 14 Drain-source on-state resistance



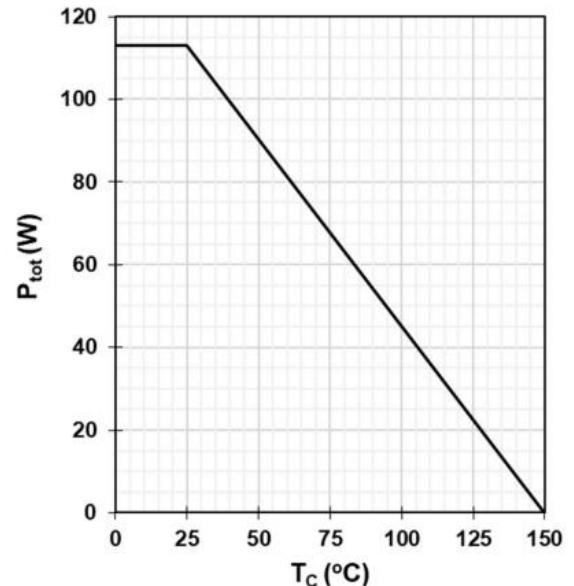
$$R_{DS(on)} = f(T_j); I_D = 5 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 15 Max. transient thermal impedance



$$Z_{thJC} = f(t_p, D)$$

Figure 16 Power dissipation

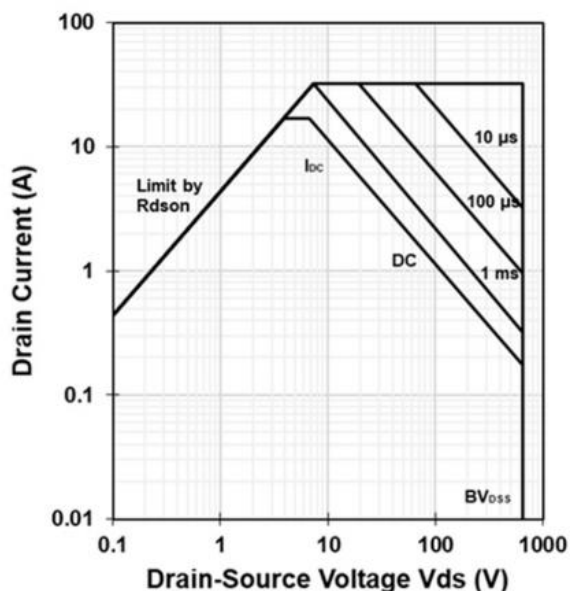


$$P_{tot} = f(T_c)$$



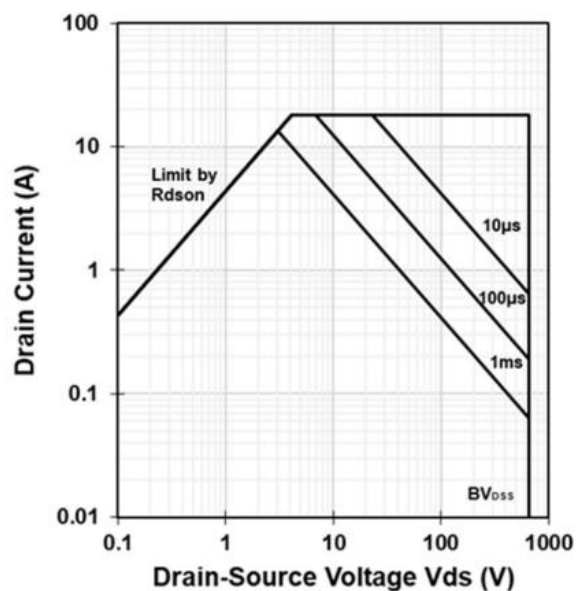
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Figure 17 Safe operating area



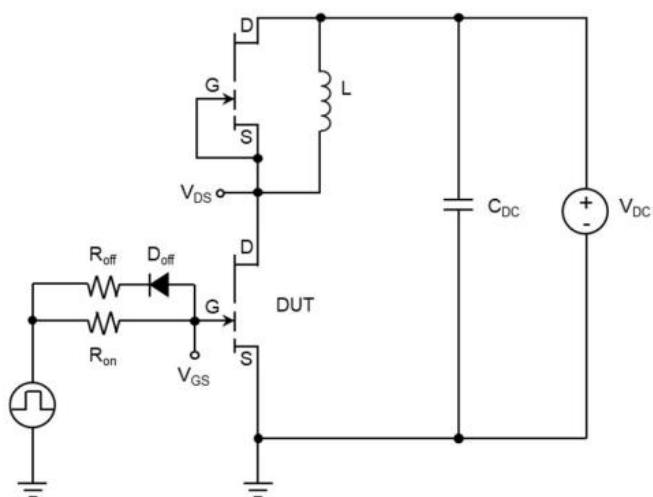
$$I_D = f(V_{DS}); T_C = 25\text{ }^{\circ}\text{C}$$

Figure 18 Safe operating area



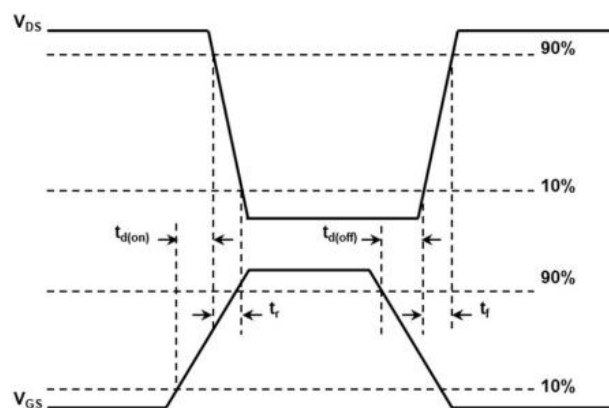
$$I_D = f(V_{DS}); T_C = 125\text{ }^{\circ}\text{C}$$

Figure 19 Switching times test circuit



$$V_{DS} = 400\text{ V}, I_D = 10\text{ A}, L = 318\text{ }\mu\text{H}, V_{GS} = 6\text{ V}, \\ R_{on} = 10\text{ }\Omega, R_{off} = 2\text{ }\Omega$$

Figure 20 Typ. switching times waveform



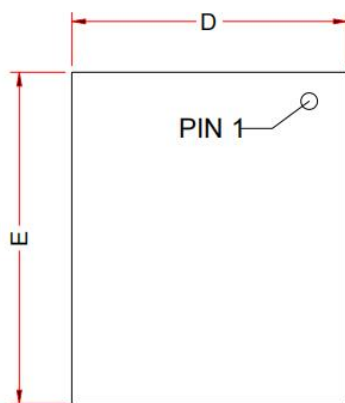


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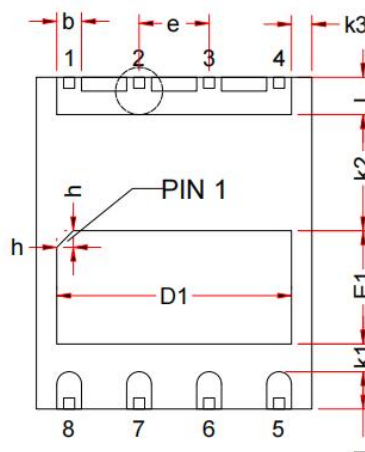
Package Information

DFN5*6

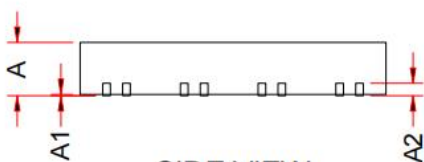
Dimensions in mm



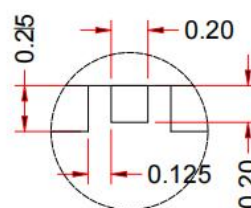
TOP VIEW



BOTTOM VIEW



SIDE VIEW



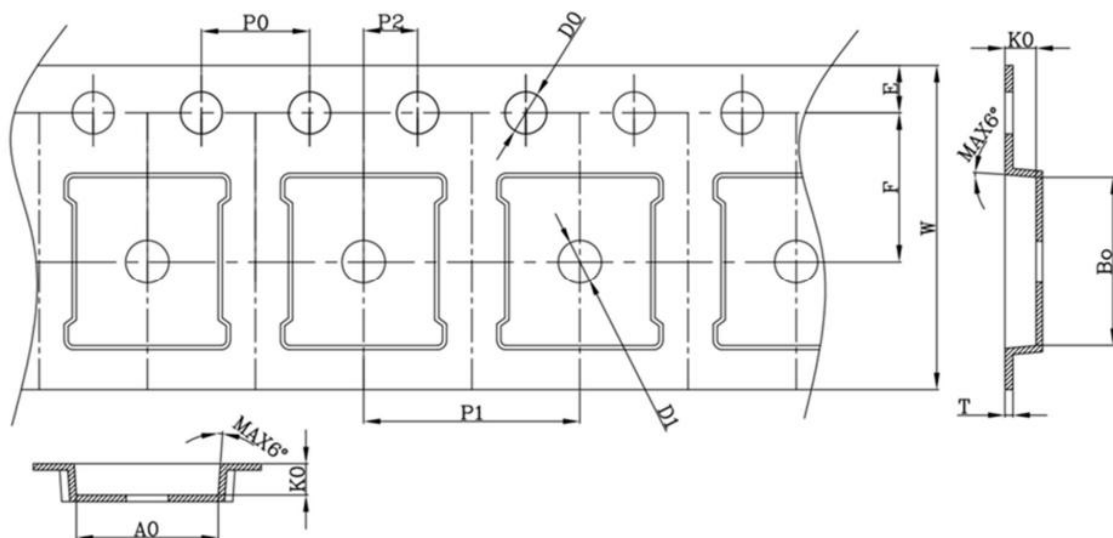
LEAD DETAIL

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.40	0.45	0.50
D	4.90	5.00	5.10
D1	4.16	4.26	4.36
E	5.90	6.00	6.10
E1	1.95	2.05	2.15
h	0.20	0.30	0.40
L	0.575	0.675	0.775
e	1.270BSC		
k1	0.400MIN		
k2	2.000MIN		
k3	0.270MIN		



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Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	12.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	8.00±0.10
F	5.50±0.05	A0	5.25±0.10
D0	1.55±0.05	B0	6.25±0.10
D1	1.55±0.10	K0	1.15±0.10
P0	4.00±0.10	T	0.25±0.05
P2	2.00±0.05		

