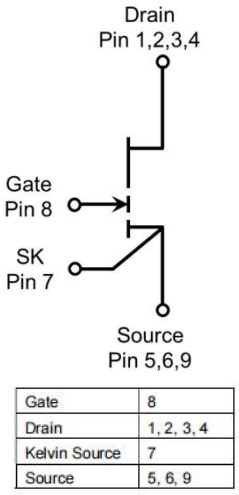
SKGM17N65-N88

Enhancement-mode GaN Power Transistor

Key Performance Parameters at T_J=25°C		
Parameters	Values	Units
V_{DS},max	650	V
$R_{DS(on)}$,max	140	mΩ
Q_G,typ	3.3	nC
I_D,Pulse	32	A
Q_{OSS},@400V	33	nC
Q_{rr}	0	nC

Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



Gate	8
Drain	1, 2, 3, 4
Kelvin Source	7
Source	5, 6, 9

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High-density power conversion
- High-efficiency power conversion

Description

650V GaN-On-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead Package (DFN) with 8 mm *8 mm Size.

Ordering Information

Type/Ordering Code	Package	Marking
	DFN 8x8 2500 pcs/reel	17N65

Absolute Maximum Ratings(at T_J = 25°C unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-source voltage	V_{DS},max	V_{GS}=0V,I_D=10μA			650	V
Drain-source voltage transient [1]	V_{DS},transient	V_{GS}=0V,V_{DS}=750V			750	V
Continuous current, drain-source	I_D	T_C=25°C			17	A
Pulsed current, drain-source [2]	I_D,pulse	T_C=25°C;V_G=6V			32	A
Pulsed current, drain-source [2]	I_D,pulse	T_C=125°C;V_G=6V			18	A
Gate-source voltage, continuous [3]	V_{GS}	T_J = -55 °C to 150 °C	-1.4		+7	V
Gate-source voltage, pulsed	V_{GS},pulse	T_J = -55 °C to 150 °C;			+10	V

		t_{Pluse}=50ns,f=100kHz;Open drain				
Power dissipation	P_{tot}	T_C=25℃			113	W
Operating temperature	T_J		-55		+150	℃
Storage temperature	T_{STG}		-55		+150	℃

1. V_{DS}, transient is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10µs.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

Thermal Characteristics

Parameter	Symbol	Notes/Test Conditions	Value	Unit
Thermal Resistance, Junction to Case, Max.	$R_{\theta JC}$		1.1	℃/W
Reflow soldering temperature, Max.	T_{SOLD}	MSL3	260	℃

Electrical Characteristics(at T_J = 25 ℃, unless specified otherwise.)

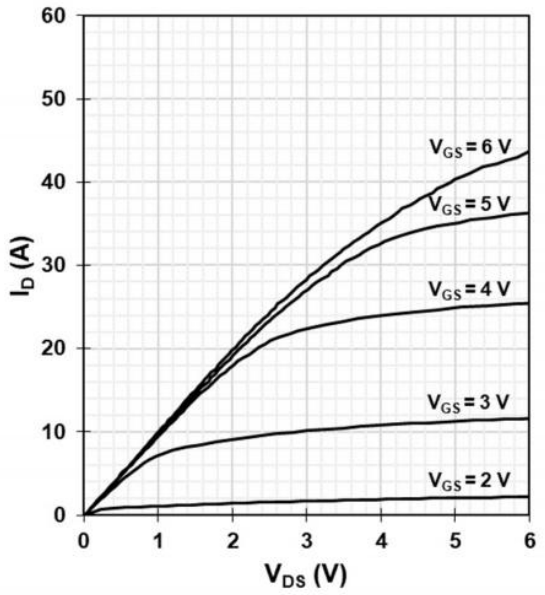
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Gate Threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=17.2mA,T_J=25℃	1.2	1.7	2.5	V
		V_{DS}=V_{GS}, I_D=17.2mA,T_J=125℃		1.6		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V,T_J=25℃		0.6	20	µA
		V_{DS}=650V,V_{GS}=0V,T_J=125℃		1		µA
Gate-source leakage current	I_{GSS}	V_{GS}=6V, V_{DS}=0V		40	200	µA
Static Drain to Source on resistance	$R_{DS(on)}$	V_{GS}= 6V, I_D=5A,T_J=25℃		100	140	mΩ
		V_{GS}= 6V, I_D=5A,T_J=125℃		200		mΩ
Internal Gate Resistance	R_G	f=5MHz,open drain		3.5		Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS}=400V,V_{GS}=0V, f=100kHz		125		pF
Output Capacitance	C_{oss}			40		pF
Reverse transfer capacitance	C_{rss}			0.5		pF
Effective output capacitance,energy related [1]	$C_{O(er)}$	V_{DS}=0V to 400V,V_{GS}=0V		53		pF
Effective output capacitance,time related [2]	$C_{O(tr)}$			81		pF
Output charge	Q_{OSS}	V_{DS}=0V to 400V,V_{GS}=0V		33		nC
Gate charge characteristics						
Gate charge	Q_G	V_{GS} = 0 to 6 V, V_{DS} = 400 V,		3.3		nC
Gate-source charge	Q_{GS}	I_D = 5A		0.3		nC

Gate-drain charge	Q_{GD}			1.25		nC
Gate plateau voltage	V_{plat}	V_{DS} = 400 V,I_D = 5 A		2.4		nC
Reverse conduction characteristics						
Source-drain reverse voltage	V_{SD}	V_{GS} = 0 V,I_{SD} = 5A		2.5		V
Pulsed current, reverse	$I_{S,pulse}$	V_{GS} = 6 V		28		A
Reverse recovery charge	Q_{rr}	I_{SD} =5 A,V_{DS} = 400 V		0		nC
Reverse recovery time	t_{rr}			0		ns
Peak reverse recovery current	I_{rrm}			0		A

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

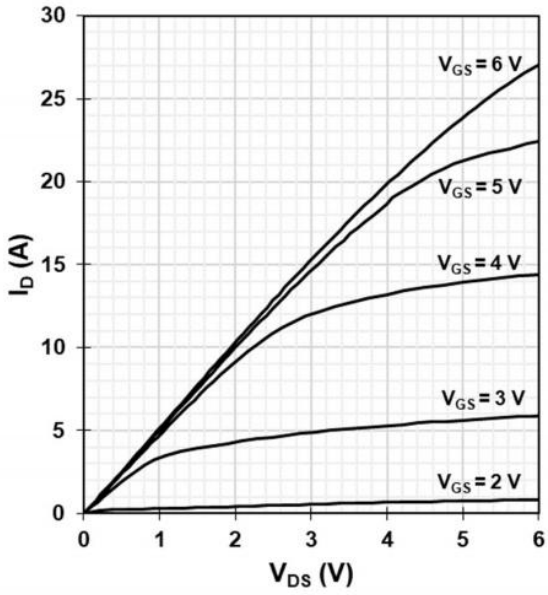
Electrical Characteristics Diagrams(at T_J = 25 °C, unless specified otherwise.)

Figure 1 Typ. output characteristics



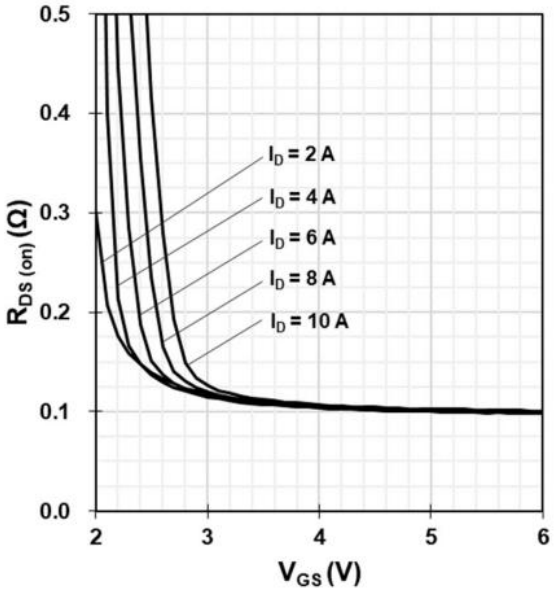
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



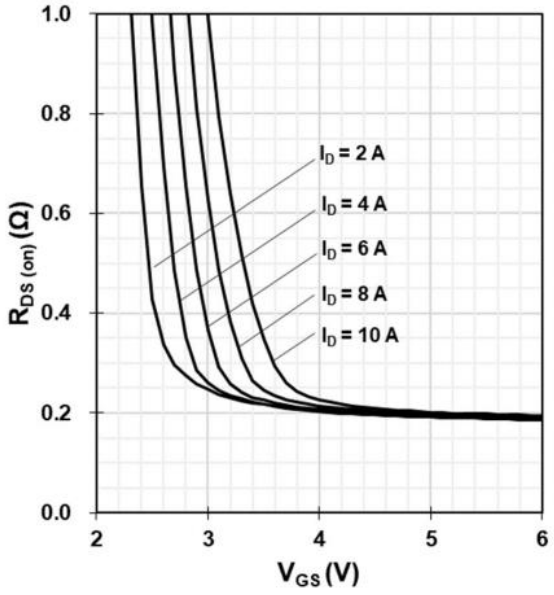
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



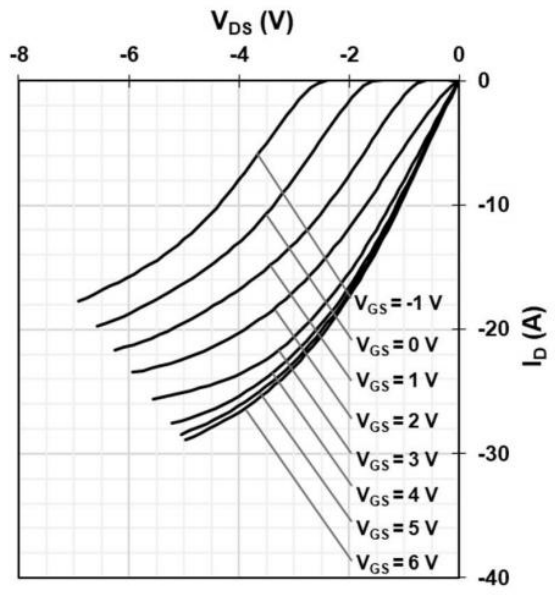
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



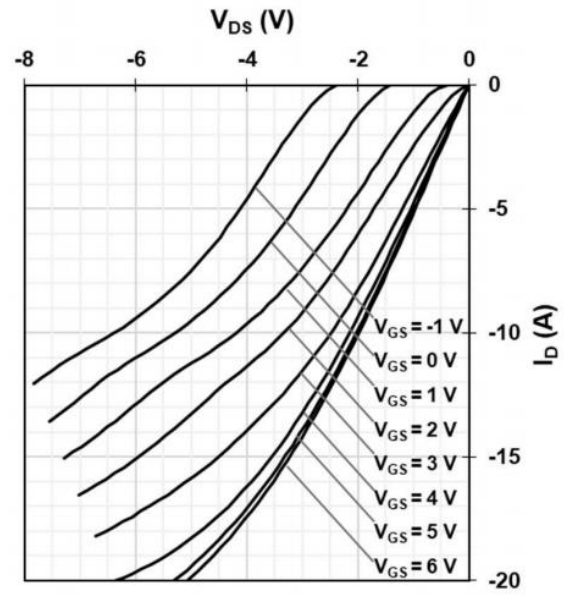
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



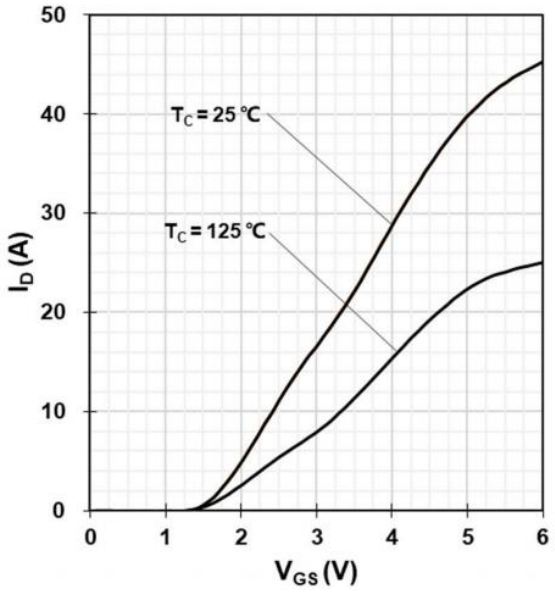
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



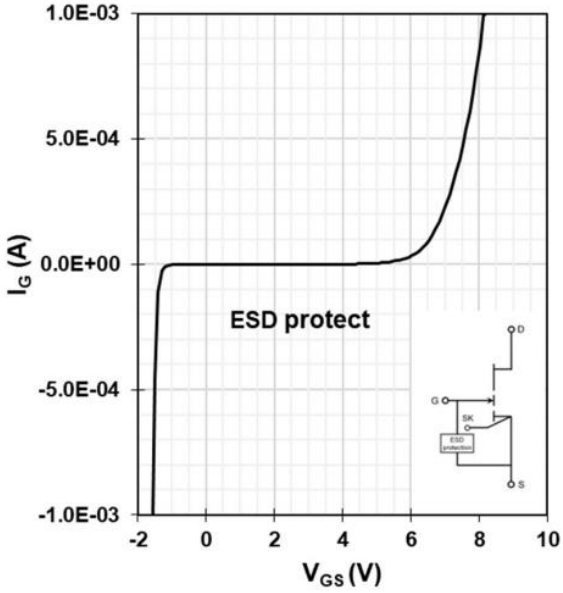
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. transfer characteristics



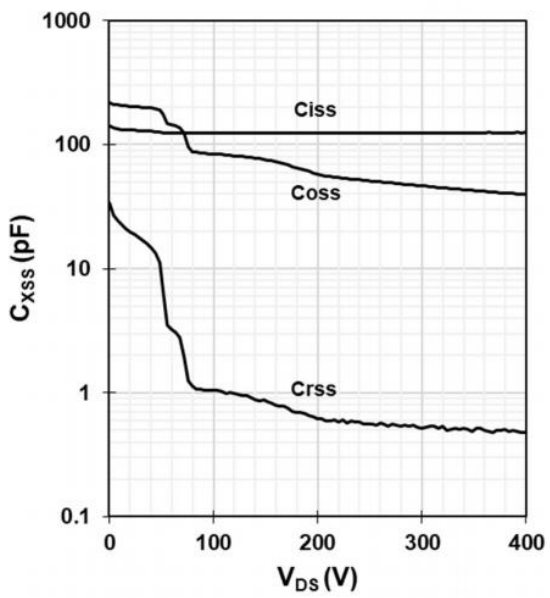
$I_D = f(V_{GS})$; V_{DS} = 5 V

Figure 8 Typ. gate-to-source leakage



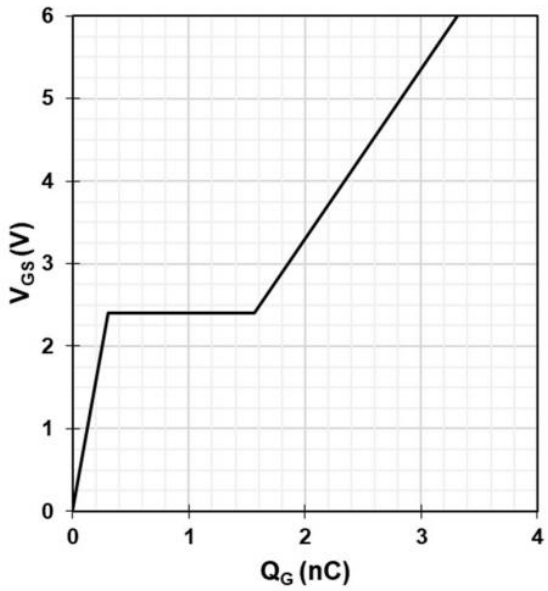
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit; V_D = open

Figure 9 Typ. capacitances



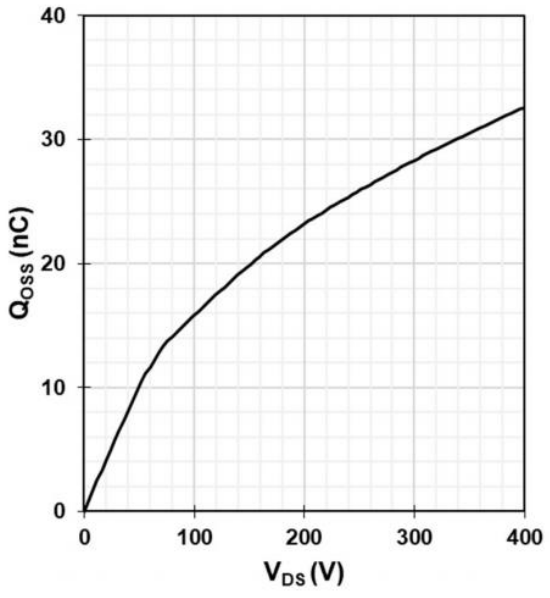
C_{XSS} = f(V_{DS}); Freq. = 100 kHz

Figure 10 Typ. gate charge



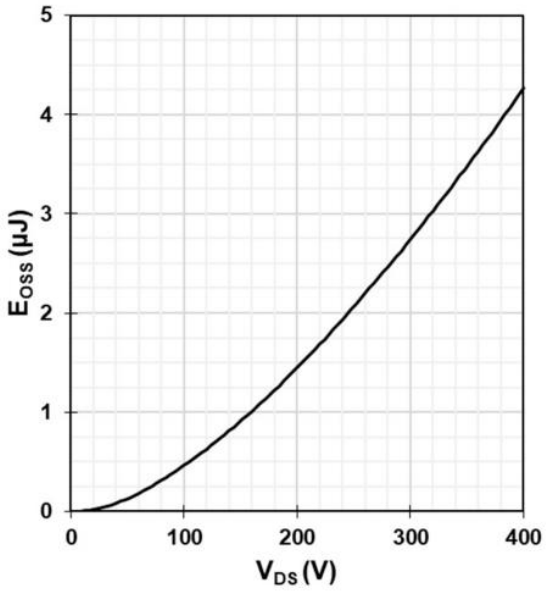
V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 5 A

Figure 11 Typ. output charge



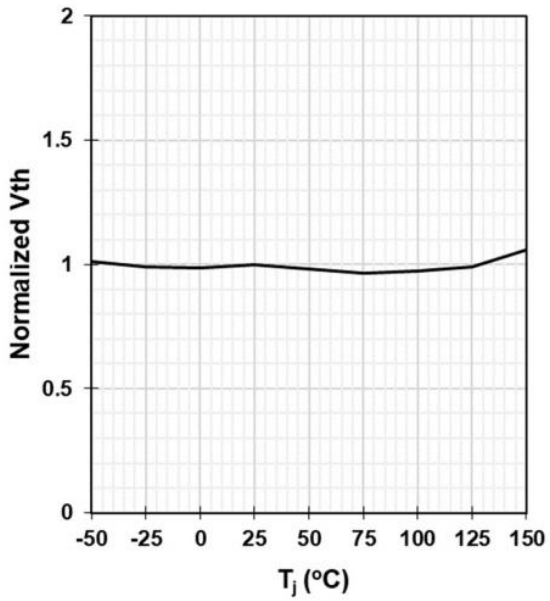
Q_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 12 Typ. C_{oss} stored energy



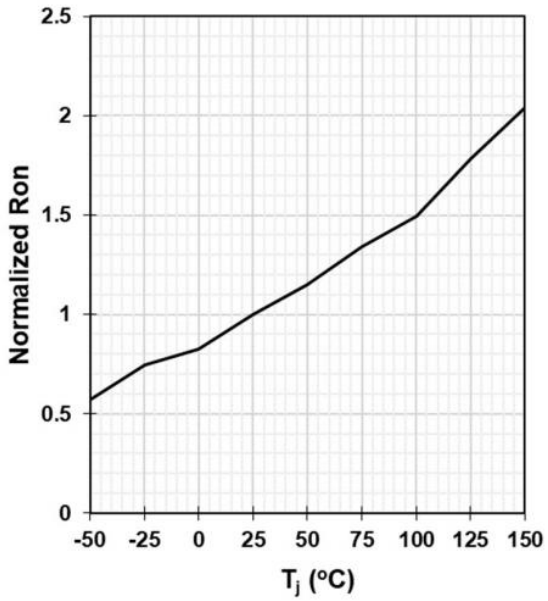
E_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 13 Gate threshold voltage



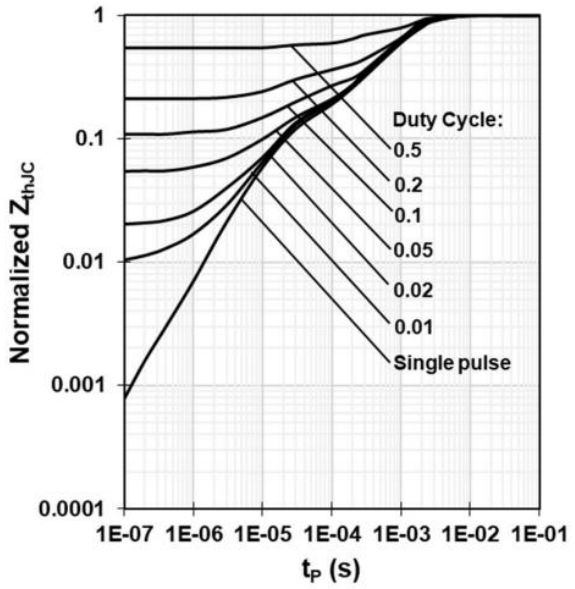
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 17.2$ mA

Figure 14 Drain-source on-state resistance



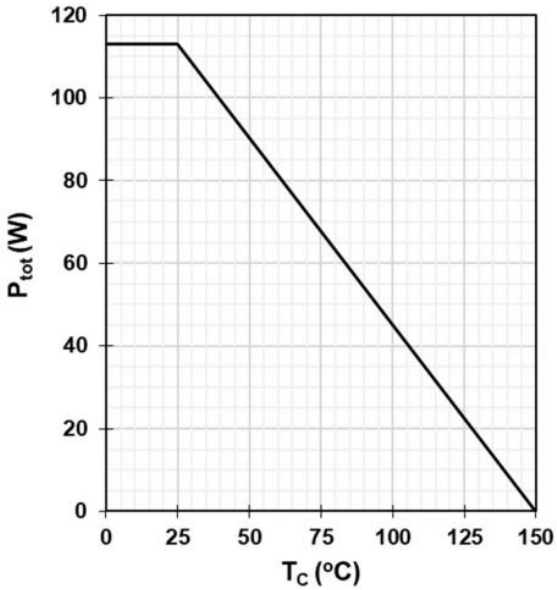
$R_{DS(on)} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 6$ V

Figure 15 Max. transient thermal impedance



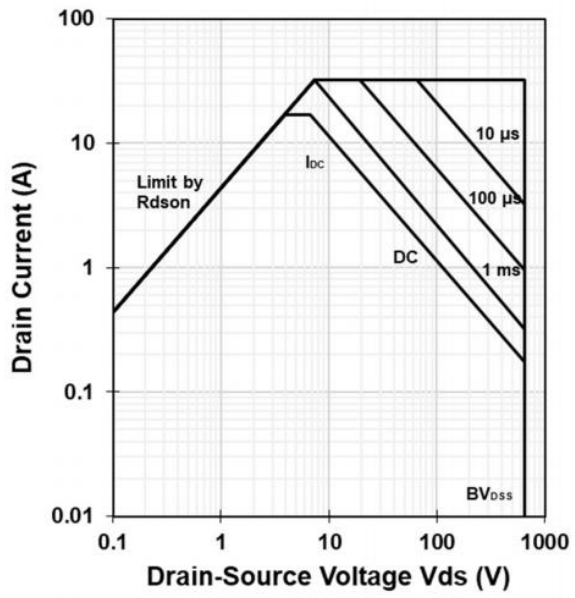
$Z_{thJC} = f(t_P, D)$

Figure 16 Power dissipation



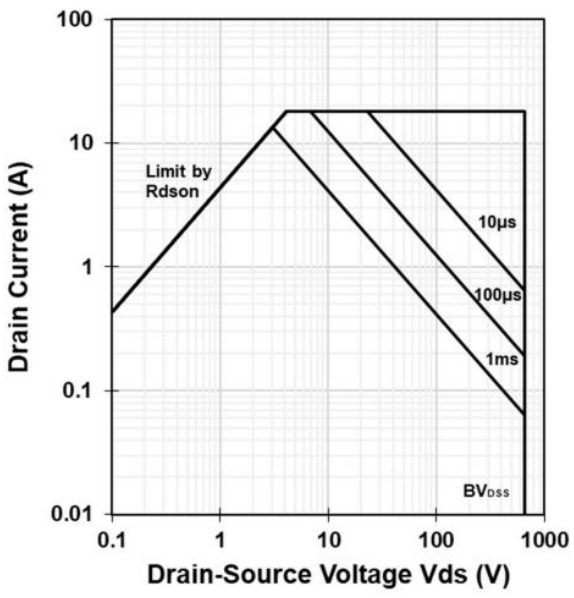
$P_{tot} = f(T_C)$

Figure 17 Safe operating area



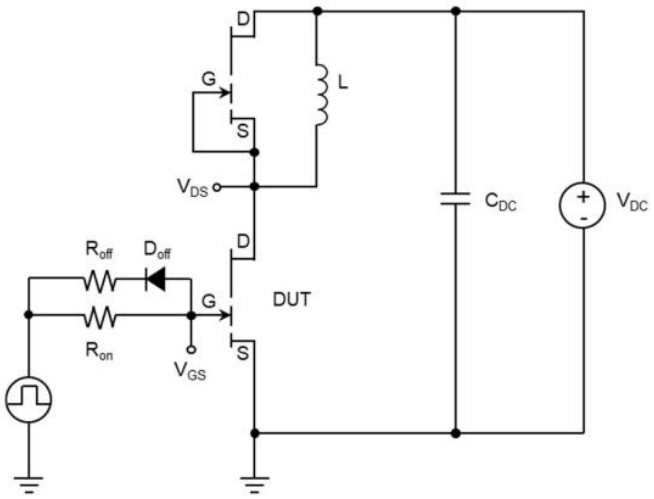
$I_D = f(V_{DS})$; $T_C = 25$ °C

Figure 18 Safe operating area



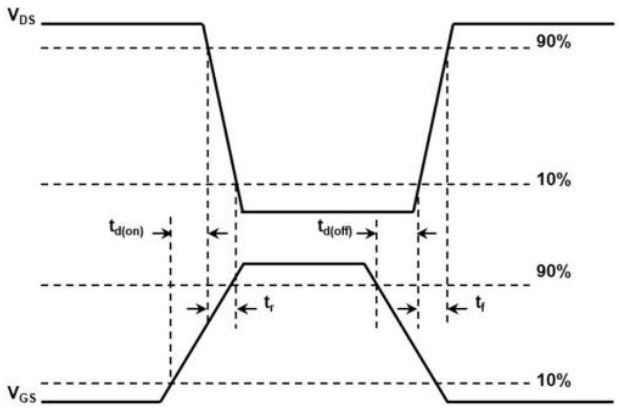
$I_D = f(V_{DS})$; $T_C = 125$ °C

Figure 19 Switching times test circuit



V_{DS} = 400 V, I_D = 10 A, L = 318 µH, V_{GS} = 6 V,
R_{on} = 10 Ω, R_{off} = 2 Ω

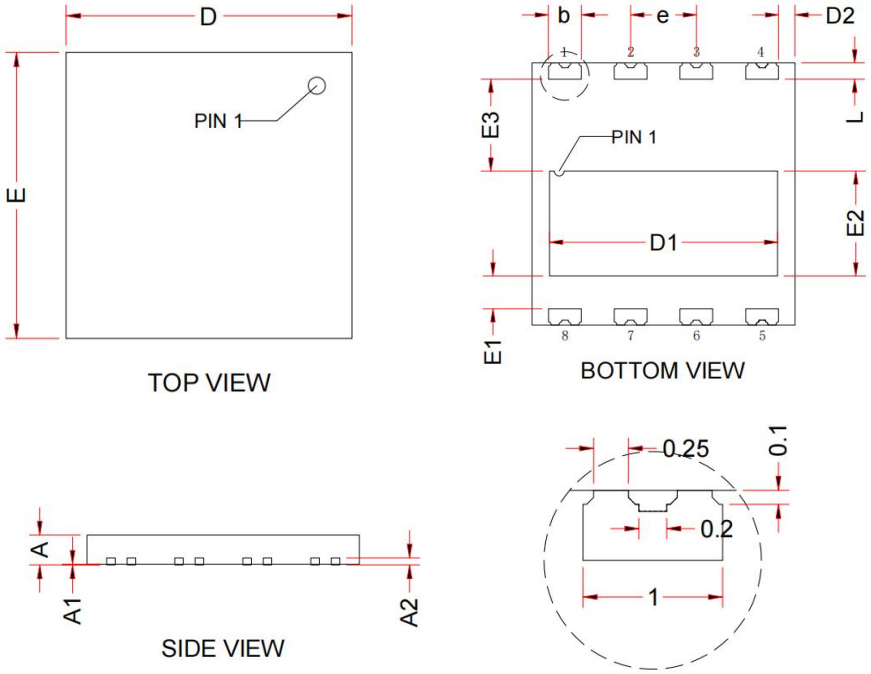
Figure 20 Typ. switching times waveform



Package Information

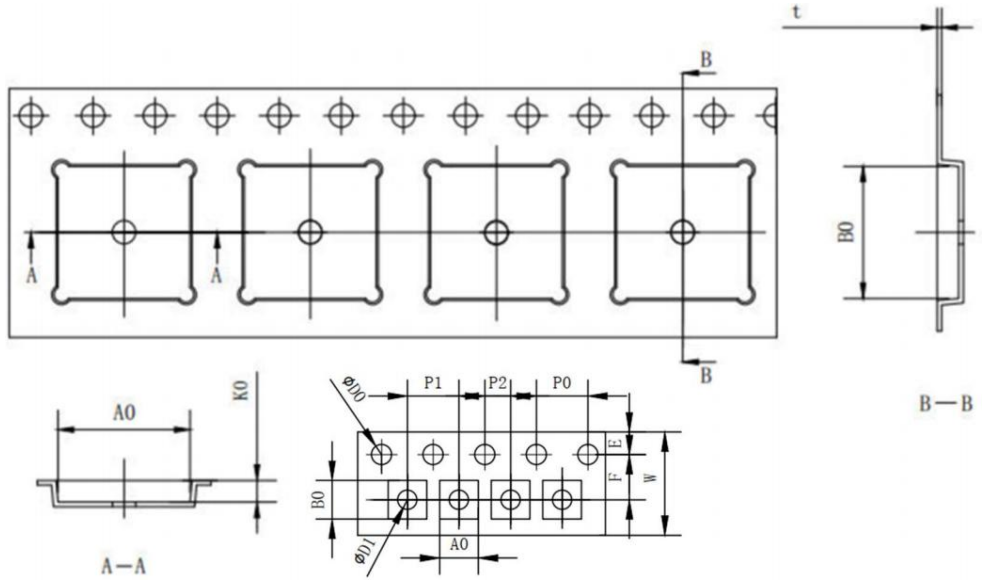
DFN8*8

Dimensions in mm



	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.95	1.00	1.05
D		8.00BSC	
D1	6.84	6.94	7.04
D2	0.40	0.50	0.60
E		8.00BSC	
E1	0.90	1.00	1.10
E2	3.10	3.20	3.30
E3	2.70	2.80	2.90
e		2.00BSC	
L	0.40	0.50	0.60

Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	t	0.30±0.05
P2	2.00±0.10