SKGI8020 Series Specifications

Advanced GaN-based Combo IC for Flyback and Boost Applications

Basic Information

1.1. General Description

The SKGI8020 series offer highly integrated solution for AC/DC conversion application with 650V enhancement -mode GaN power transistor, 650V green way startup switch as well as tailored regulated mode and versatile protect function. This economic and efficient solution can supply up to 70W on flyback and 100W on boost application.

SKGI8020 yields stable operation at 100~500 kHz high frequency to shrink transformer and output capacitor, therefore the module size and weight is significantly reduced, and power density is much higher than the traditional switching power.

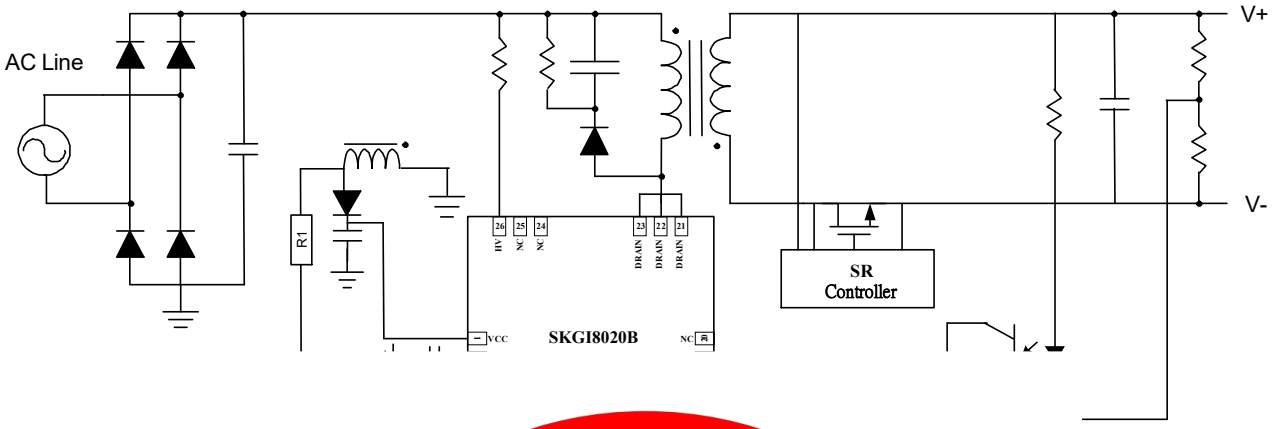
1.2. Features

- Integrated 165 mΩ(SKGI8020B165) or 365mΩ (SKGI8020B365) GaN transistor
- Integrated startup switch
- Switching frequency up to 500 kHz
- Valley-switched for better efficiency and EMI
- Minimal BOM cost and component count
- Low standby power

1.3. Applications

- USB type-C power adapters
- Cell-phone and tablet chargers
- Laptop adapters
- Consumer electronics

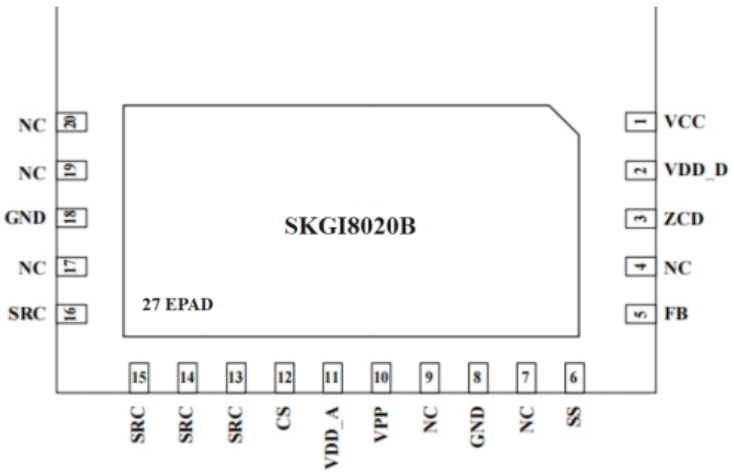
1.4. SKGI8020 Simplified Application Diagram



2. Pin Con

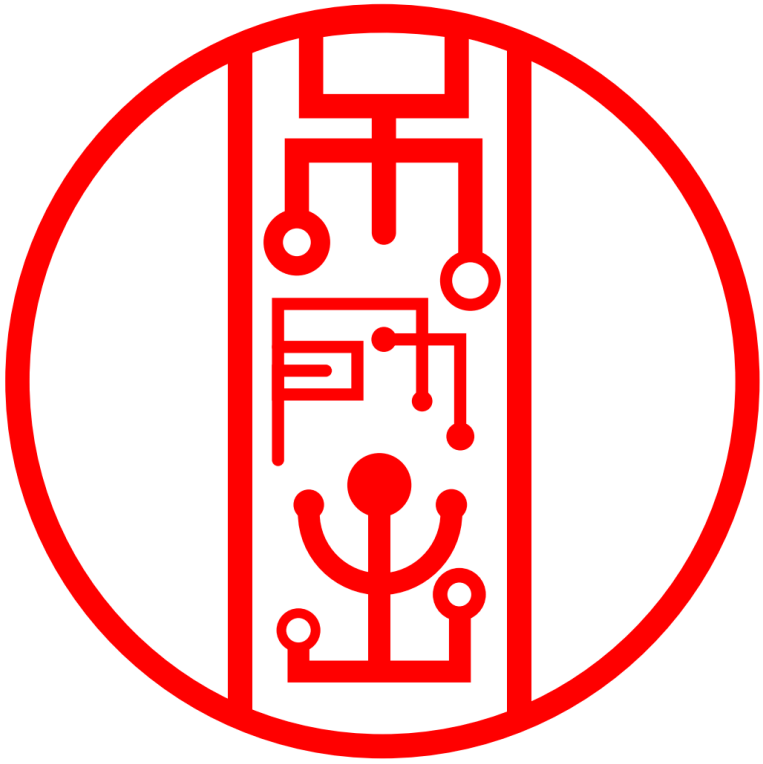
2.1.

- SKGI802



■ Pin Name and Number (SKGI8020B)

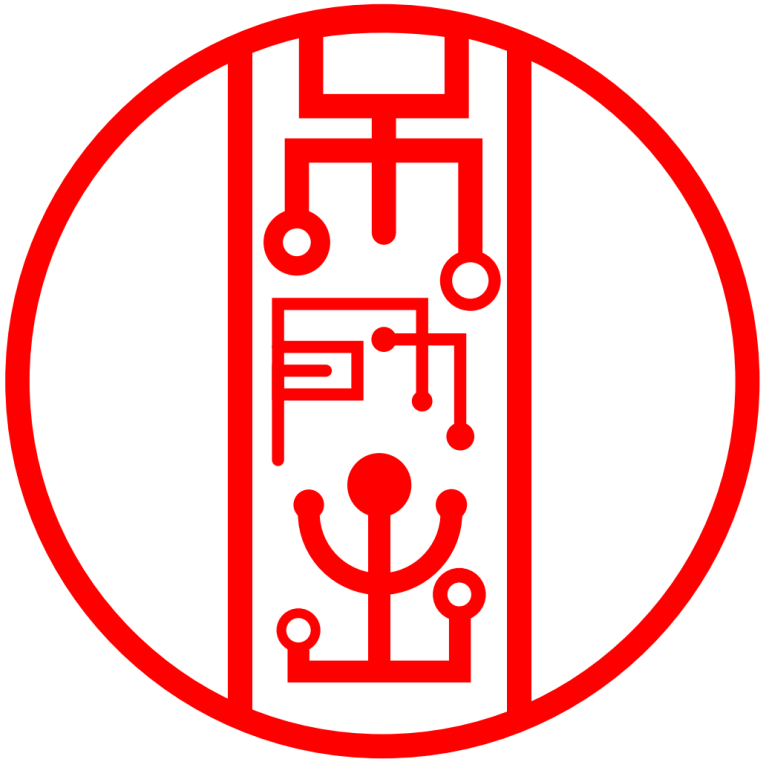
Pin No. \ Pin Name	SKGI8020B
1	VCC
2	VDD_D
3	ZCD
4	NC
5	FB
6	SS
7	NC
8	GND
9	NC



2.2. Pin Des

Ver. B Index	Pin	
1		CC exceeds Vcc,off. After
2	VDD_D	**Reference power pin for driver stage**
3	ZCD /Pulse	(**SKGI8020**)**Zero current detection pin.** A resistor divider from the auxiliary winding to this pin provides information of demagnetization to control the power transistor switching. The pin is also for primary over voltage protection (POVP) and brown out (BO) protection while DRV is high. The pin also provides secondary side output protection (SOVP) while DRV is low.
5	FB	**Feedback pin from Opto-isolator.** The pin refers to an internal bias, VDDA with an external resistor, R_{fb}. The switching frequency, CS pin peak voltage and burst mode are related to the pin.
6	SS	**Soft-start pin.** a capacitor is connected for entering steady state operation gradually.

Ver. B Index	Pin Name	Function Description
8,18	GND	**Ground pin.**
10	VPP	**Test pin.** Short to VDD_A pin in normal operation
11	VDD_A	**Analog power pin.**
12	CS	**Current sensing pin.** Cycle−by−cycle current limiter.
13,14, 15,16	S	
21,22,23	D	
26		
4,7,9,17, 19,20,24, 25		
27	E	



2.3. Part Nu

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SKGI8020

2.4. Switchi

Pa		Frequency in (KHz)
SKGI8020B165/365-1	160	50
SKGI8020B165/365-0	95	

2.5. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage	650	V
V_{CC}	Supply Voltage	30	V
Vzcd	Auxiliary Sense Voltage	6	V
I_D	Drain Current (continuous) at TC = 25°C Single Operation SKGI8020B165 SKGI8020B365	22 11	A
	Drain Current (continuous) at TC = 125°C Single Operation SKGI8020B165 Sk	15	A
I_{DM}	Dr Sk Sk		A
P_{tot}	Tc		W
	Tc		W

2.6. Thermal

Symbol		Unit
$R_{th,jc,B}$	Ther	°C/W
$R_{th,ja}$	(*)Th	°C/W
T_j	Ther	°C
T_{stg}	Stor	°C

2.7. Electrical Characteristics (Startup HEMT)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage (Startup HEMT)	I_D = 250 μA,	650			V
I_{DSS}	Off State Drain Current (Startup HEMT)	V_{DS} = Max Rating T_C = 25°C			100	μA
		V_{DS} = Max Rating T_C = 125°C			200	μA
I_{GSS}	Gate-Source Leakage Current (V_{DS} = 0) (Startup HEMT)	V_{GS} = ± 20 V			500	nA
$V_{CC,on}$	Unde turn-				16	V
$V_{CC,off}$	Unde turn-				8	V
$I_{cc,q}$	Quie				100	μA
$I_{cc,op}$	Oper				4	mA

Unless noted, Vc

2.8. Dynamic

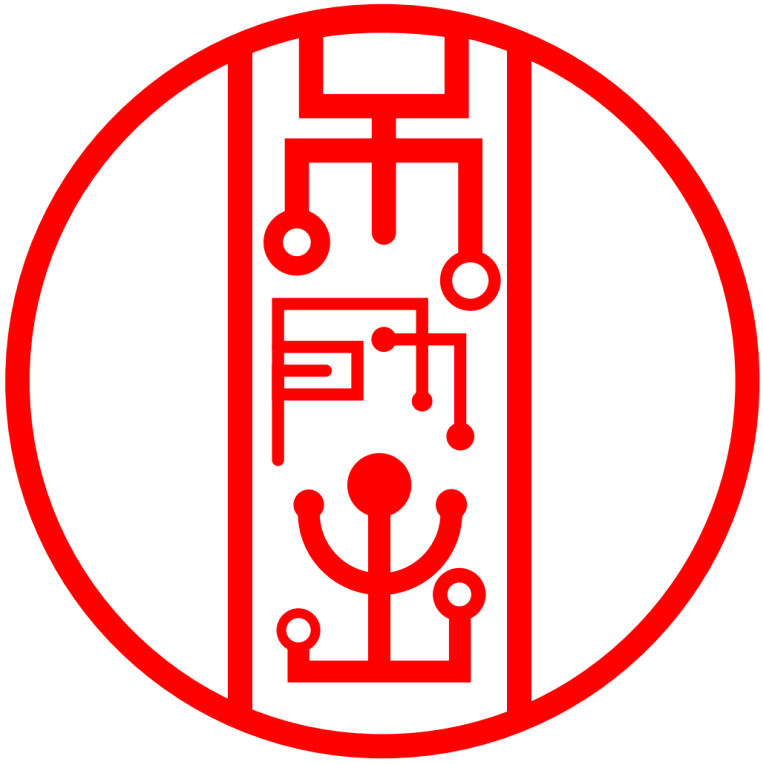
Symbol					Max.	Unit
$C_{oss,}$	Out SKC					pF
$C_{oss,}$	Out SKC					pF
$Q_{oss,}$	Out SKG					nC
$Q_{oss,}$	Out SKG					nC
f_{sw-max}	Max (SK				603 198 105	kHz
f_{sw-min}	Max. Switching Frequency (SKGI8020B165/365-0/1/2)	ZCD tie to GND Vfb=4V	45	50	84	kHz
$f_{sw,burst}$	Burst Mode Frequency	at cutoff		20		kHz

2.9. Controller Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CC,bias}$	Startup bias voltage	V_{IN} = 100V		15		V
t_{LEB}	Current sense leading-edge blanking	Vcs=0.8V	60	100	150	ns
V_{FB}	Feedback bias voltage		4.5	5	5.5	V
R_{FB}	Fee				(20) 35	kΩ
$V_{FB,burst}$	Fee burs				1.1	V
$f_{sw,range}$	Fre setp				150	%
$V_{Ipk,max}$	Cur max				0.65	V
$V_{Ipk,min}$	Cur min				0.17	V
t_{SS}	Soft				5	ms
Iss	Sou Soft				110	μA
$t_{ZCD,pd}$	ZCD swit				50	ns
$f_{D,zcd}$	Dra (val				10	MHz

2.10. Fault Protection

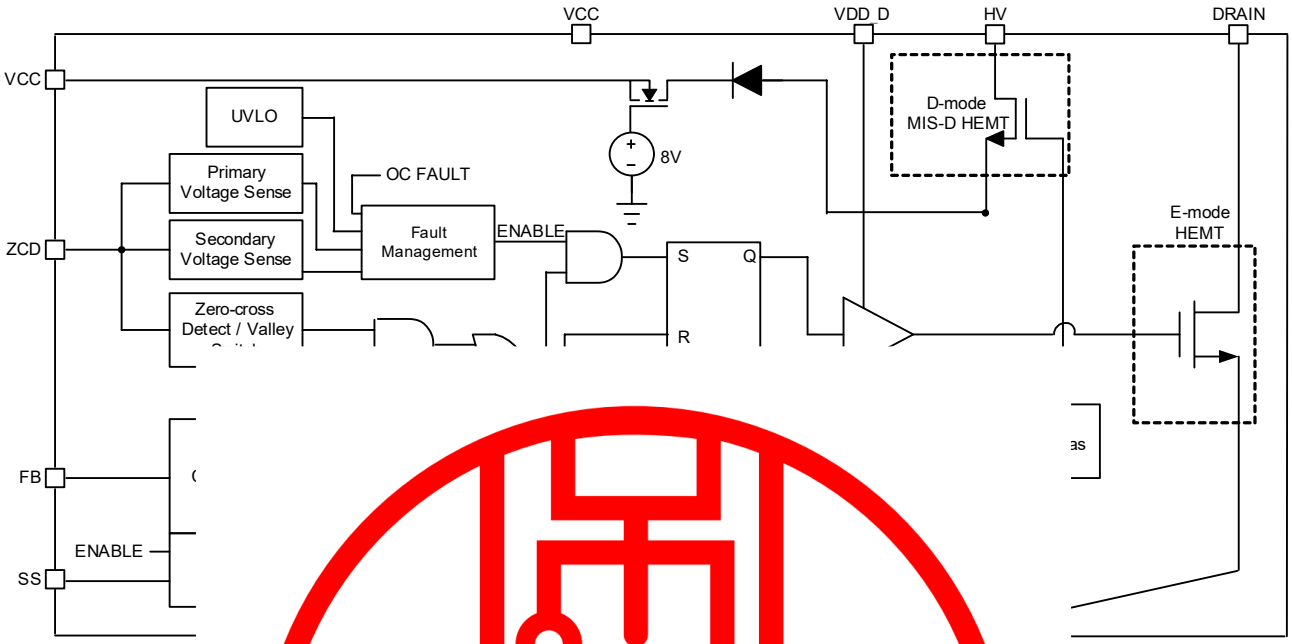
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{zcd,BO}$	Brown-out threshold, ZCD-referred current	ZCD PAD link 50Kohm Resistor. Given negative voltage to the other end of the resistor.	100	110	120	uA
$I_{zcd,POVP}$	Primary overvoltage threshold, ZCD-referred current	ZCD PAD link 50Kohm Resistor. Given negative voltage to the other end of the resistor.	466	486	506	uA
$V_{zcd,SOVP}$	Secondary overvoltage thre				3.3	V
$t_{zcd,P}$	ZCI prim				250	ns
$t_{zcd,S}$	ZCI sec				350	ns
$t_{BO/OVP}$	Bro prot					us
V_{OCP}	Ove thre					V
$t_{LEB,OCP}$	OCI				150	ns
$t_{OCP,LO}$	OCI					ms



2.11. Internal [illegible]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_r	Rising Time	Cload=50pF, V_{OH} = 4.5V,V_{OL}=0.5V f_{sw} = 400KHz	1	2	5	ns
T_f	Falling Time	Cload=50pF, V_{OH} = 4.5V,V_{OL}=0.5V f_{sw} = 400KHz	1	2	5	ns

2.12. Simplified Internal Block Diagram



2.13. Detailed Description

SKGI802x, the GaN integrated IC, is for low-side power transistor use applications , such as the flyback, forward, boost, and inverted buck topologies . An integrated GaN FET and startup switch yields an economic and easy-to-use solution.

2.14. Startup Bias

Green way startup is realized by D-mode transistor. A bias current keeps startup transistor conducting until VCC exceeds UVLO level, the startup transistor turns off to meet green requirement when system is in stand-by mode while IC is supplied by auxiliary winding.

2.15. Peak Cu

The SKGI802x
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2.16. Control

The SKGI 802(
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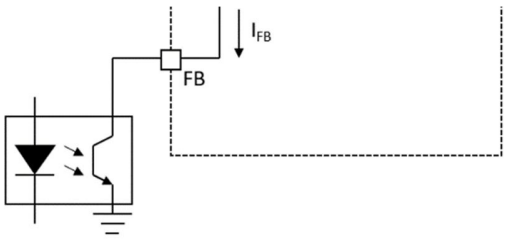


The control law generates the desired frequency and peak current limit as a function of this feedback current. This relationship is shown below:

The control law is chosen to keep the switching frequency at the target value at higher loads and decrease the switching frequency at lighter loads. Peak current will likewise decrease as load decreases. To improve EMI performance, peak current levels will first decrease before switching frequency falls to the range of F_{min} to F_{max} to improve EMI filter size.
The slopes of the peak current and switching frequency values, with respect to feedback pin current, will determine the gain of the system. It is designed for the gain to track the switching frequency to reduce bandwidth and maintain stability at lighter loads. Careful design of the control law circuitry is needed to create a smooth gain curve with the desired characteristics.

2.17. Soft-Start

The SKGI802x includes a flexible soft-start function to support external primary-side and secondary-side controllers . A capacitor from SS to GND will determine the soft-start rate of the converter . Before the UVLO threshold is reached , or during faults , the SS capacitor is discharged to ground , and the soft- start latch is reset. When the UVLO and any faults clear, an internal resistor charges the SS capacitor from an internal VDDA supply. The soft-start pin voltage is following relationship:

$$V_{ss}(t) = \frac{I_{ss}}{C_{ss}} t,$$

where I_{ss} is the sourcing current from SS pin and C_{ss} is the external capacitor connecting to SS pin. When soft-start begins, the control law will use V_{ss} as this equivalent feedback voltage $V_{FB,eq}$. When V_{FB} falls below V_{ss}, the soft-start process finished and the control law follows V_{FB}. Once this occurs, the soft-start is latched off and the control law will follow V_{FB} until a UVLO or fault event occurs.
The soft-start can be manipulated by changing the external SS capacitor or adding an external charge or discharge path. If a secondary-side controller is used, the soft-start ramp must be sufficiently slow to allow the secondary-side controller to start before the output voltage overshoots. The converter can be disabled temporarily by discharging the SS capacitor externally.

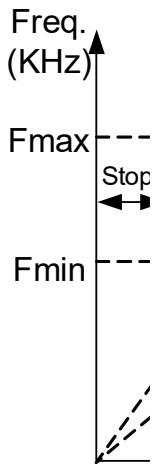
2.18. Oscillator and Gate Switching

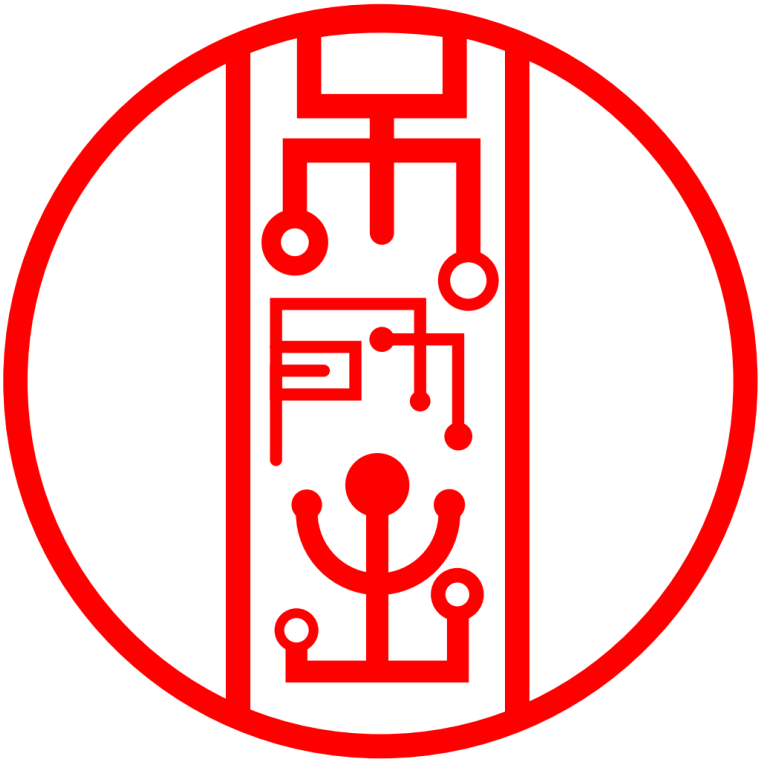
The SKGI802x operates at a variable switching frequency to enable valley switching at different loads to improve efficiency. The switching frequency is constrained within a range to ensure switching losses and EMI are well controlled among different loads.

The control law produces a current proportional to the desired switching frequency. This current charges an internal timing capacitor. The timing capacitor is discharged to ground at the beginning of each switching period when the primary-side transistor is turned on. Two comparators are used to determine the minimum and maximum switching frequency (or maximum and minimum period, respectively). The minimum frequency comparator uses a threshold voltage of 1.5V, while the maximum frequency comparator uses a threshold voltage of 0.8V. (*Dev Note: These thresholds and oscillator implementation can vary based on implementation preferences*).

The next switc imum frequency comparator is t no valleys have been detected.

The relationsh are as following diagram.





The next switc imum frequency comparator is triggered, or when the minimum frequency comparator is triggered if no valleys have been detected. The maximum and minimum frequencies are shown as the table in Sec.2.3. If FB is lower than around 1V, the DRV stops and system goes into burst mode.

2.19. Valley Detection

A zero-crossing detection circuit is used to sense the zero-crossing of the transformer auxiliary voltage. This zero-crossing is used to switch the primary-side transistor at the valley of the drain voltage waveform, reducing switching losses and improving efficiency.

As the SKGI8020 utilizes a GaN transistor and features a lower-inductance transformer, the drain ringing will be faster than a traditional flyback converter. The internal propagation delay of the zero-cross circuit will shift the switching edge to the valley. In converters where the ringing is slower, a small

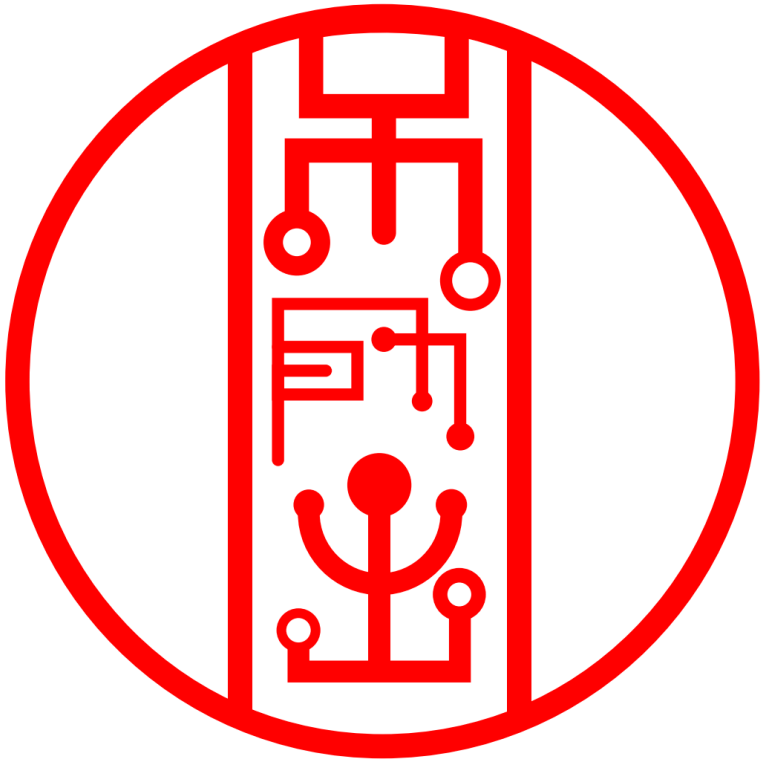
capacitor can be added to the VS pin to delay the sensed signal.

2.20. Primary-Side and Secondary-Side Voltage Detection

The primary-side voltage is sensed from the VS pin while the primary-side switch is on. As the auxiliary voltage is negative while the primary-side switch is on, a common-gate amplifier is used to reconstruct a positive version of this signal in the IC. The reconstructed signal is proportional to the current out of the VS pin needed to bring the VS pin to ground, designated as I_{VS}. The VS resistor network can be adjusted to yield the desired brownout and OVP thresholds.

The secondary-side voltage is sampled from the VS pin shortly after the primary-side switch turns off. It is compared oltage event has occurred.

The primary-si ndependently by configuring the X winding to VS, and R2 is the re oltages be $V_{IN,MIN}$ and $V_{OUT,MAX}$, re urns count np, ns and na respect The secondary



Likewise, the ir

To determine t value of R1, then use the first eq

2.21. Fault Management

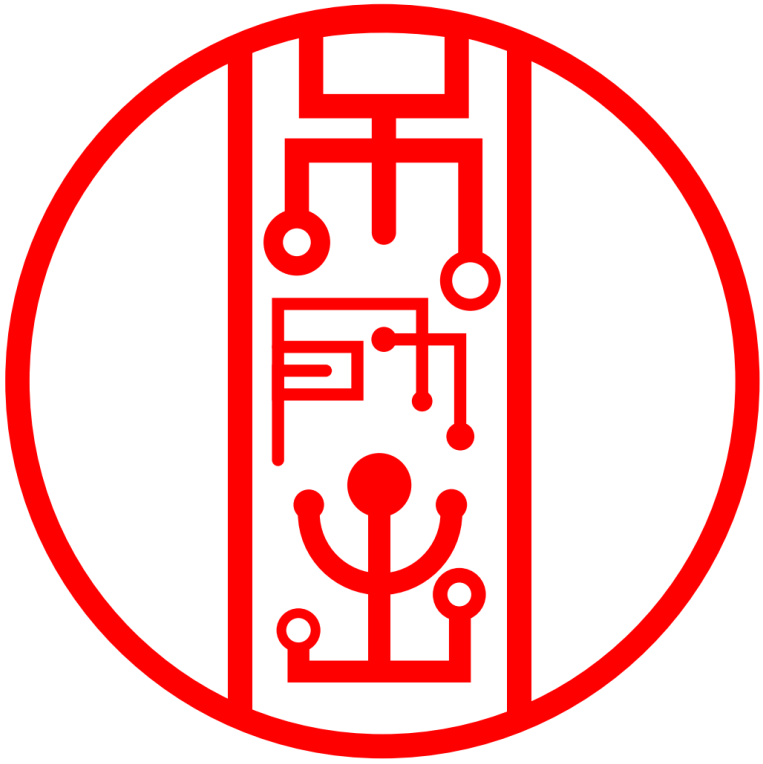
The SKGI802x responds to various faults in the system to protect the converter against internal and external fault conditions. The SKGI802x includes protection against VCC undervoltage, primary-side brownout and overvoltage, secondary-side overvoltage, and primary-side overcurrent.

VCC undervoltage (UVLO) is continually monitored by the UVLO circuit. A significant hysteresis is used to enable startup via the low-current bias supply. The VCC capacitor will discharge during startup until the output and auxiliary voltage supports charging the capacitor. The converter will immediately shut off when a UVLO event occurs and will undergo a soft-start when the UVLO condition is cleared.

Primary-side brownout and overvoltage (POVP) protection uses the sampled primary-side voltage from the auxiliary voltage. The converter must be switching to refresh this measurement; this protection is not active until the converter begins switching. When a brownout or POVP condition occurs, the converter shuts off for a 100 us period. After this period expires, the converter will undergo a soft-start, including primary voltage monitoring. A repeated brownout or POVP condition will yield a 10 kHz hiccup rate.

Secondary-side overvoltage (SOVP) protection uses the sampled secondary-side voltage from the auxiliary voltage. The converter must be switching to refresh this measurement; this protection is not active until the converter begins switching. When a SOVP condition occurs, the converter shuts off for a 100 us p t-start, including secondary volta frequency.

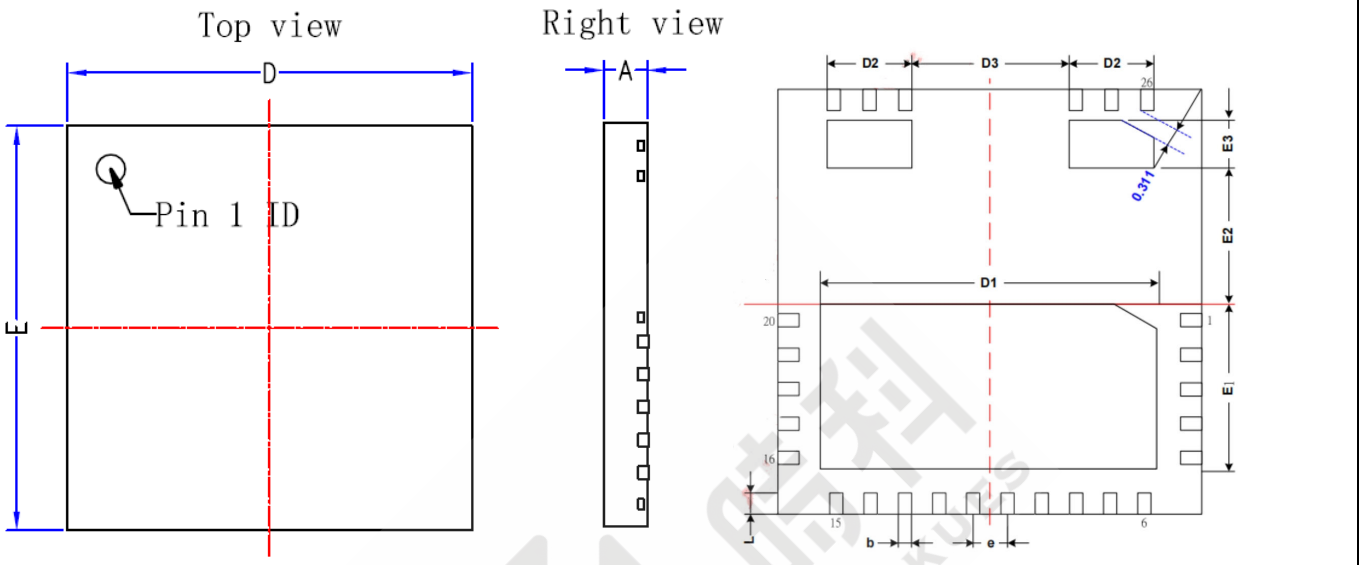
The primary-si sed primary-side switch current. . Once the OCP period expires,



3.

3.1. Package Summary

- QFN 8x8



Top View Side View Bottom View

Outline and Dimensions

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.75	0.85	0.95	**E**		8.00BSC	
b	0.20	0.25	0.30	**E1**	3.05	3.15	3.25
D		8.00BSC		**E2**	2.50	2.60	2.70
D1	6.30	6.40	6.50	**E3**	0.80	0.90	1.00
D2	1.50	1.60	1.70	**e**		0.65BSC	
D3	2.90	3.00	3.10	**L**	0.30	0.40	0.50
Primary EPAD (D2-E3 Comer):27°+ 3°							
Secondary EPAD (Center Area): 45°+ 39°							